UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :None Installed
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CRV:Chief River

BOM

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Title: *Cover Page*		
Size: A3	Document Number: LG4858L	Rev: SB
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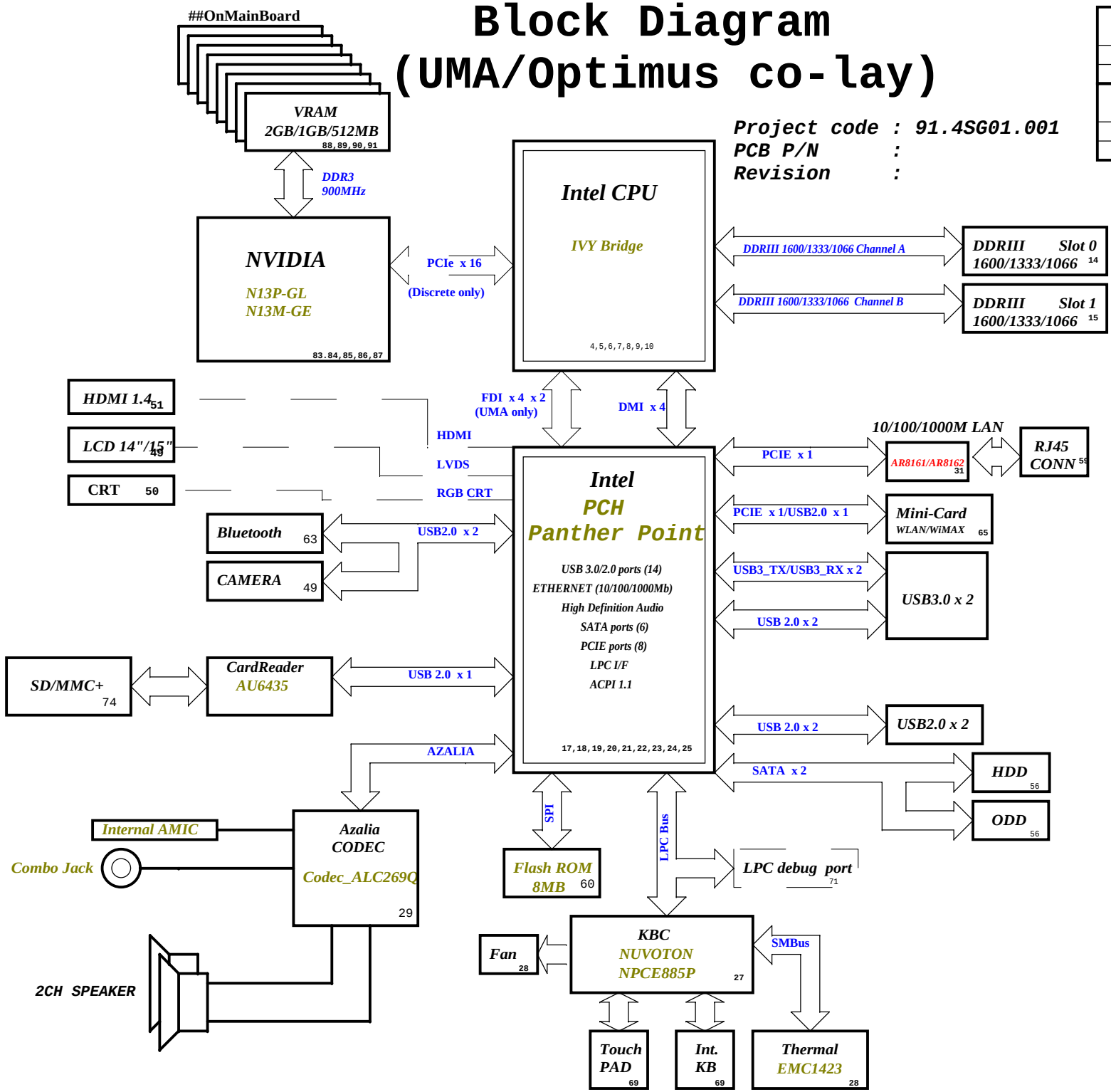
Block Diagram (UMA/Optimus co-lay)

##OnMainBoard

Project code : 91.4SG01.001
PCB P/N :
Revision :



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	VCCSA

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC G977F 45	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA ISL62882C 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24745 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

VGA switchs 93	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

All Not update

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	N/A
1	HDD1
2	N/A
3	N/A
4	ODD

USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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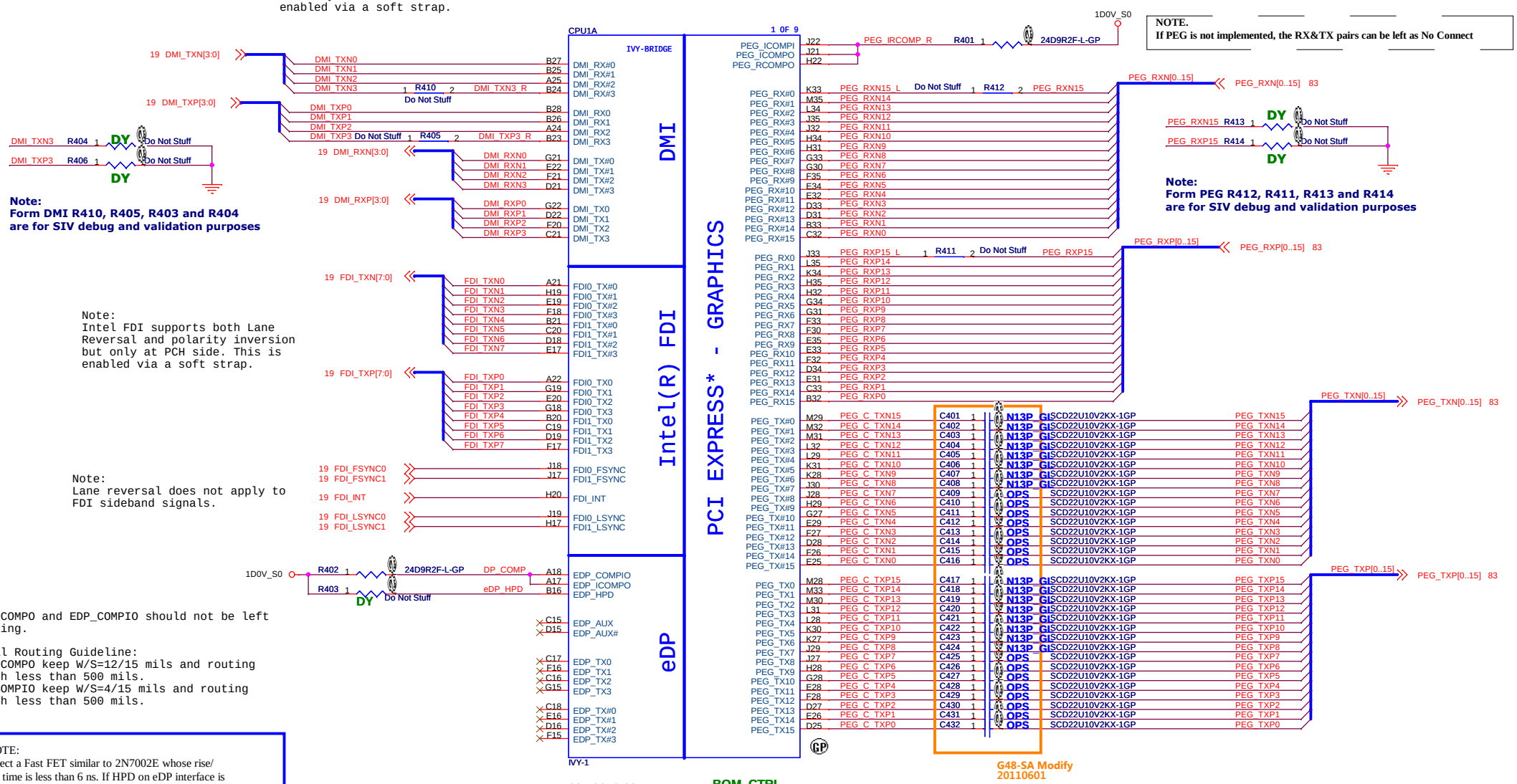
SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

62.10040.821

1st = 22.10252.171

2nd = 62.10040.821

3rd = 62.10055.551

BOM_CTRL

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Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number LG4858L	Rev SB
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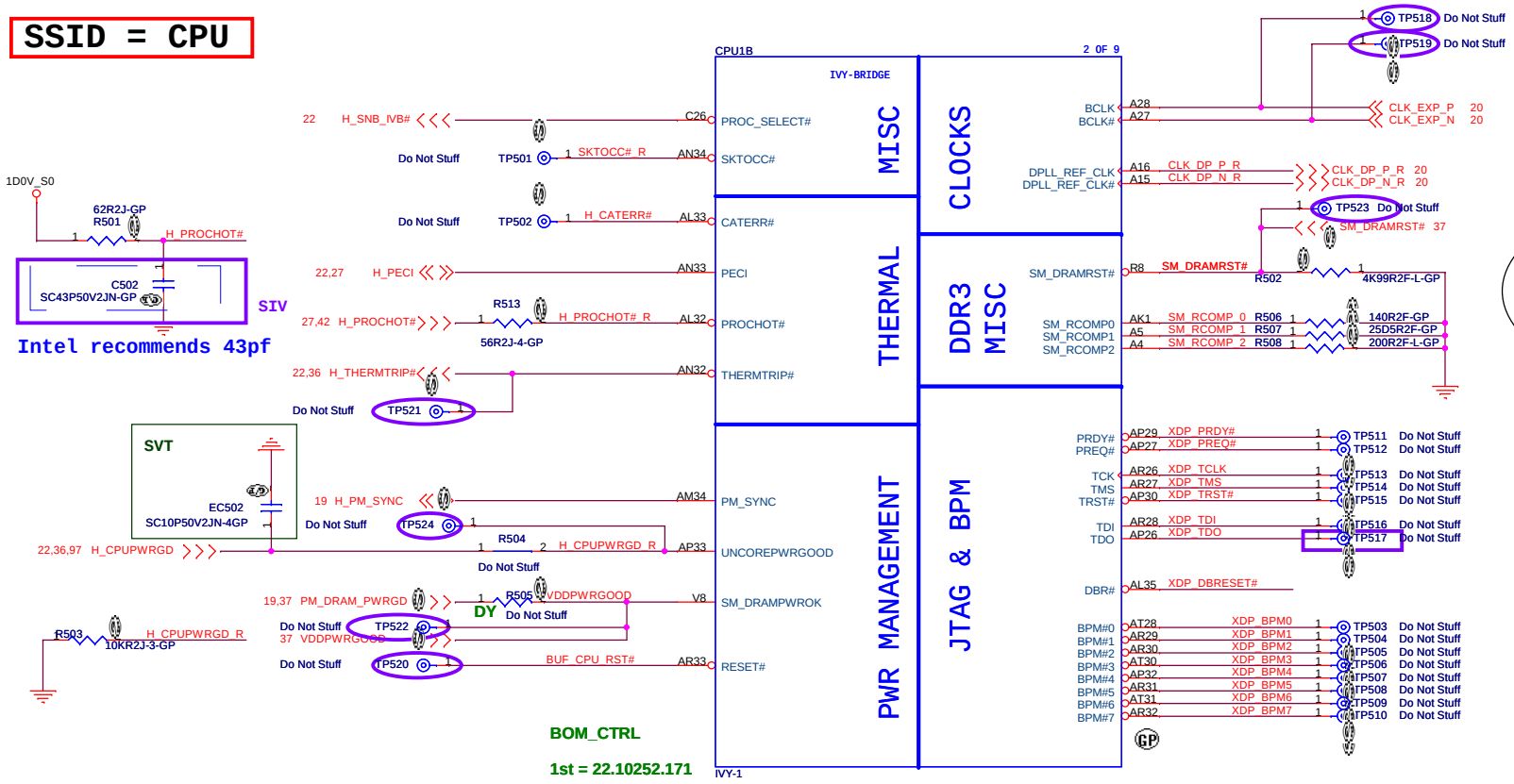
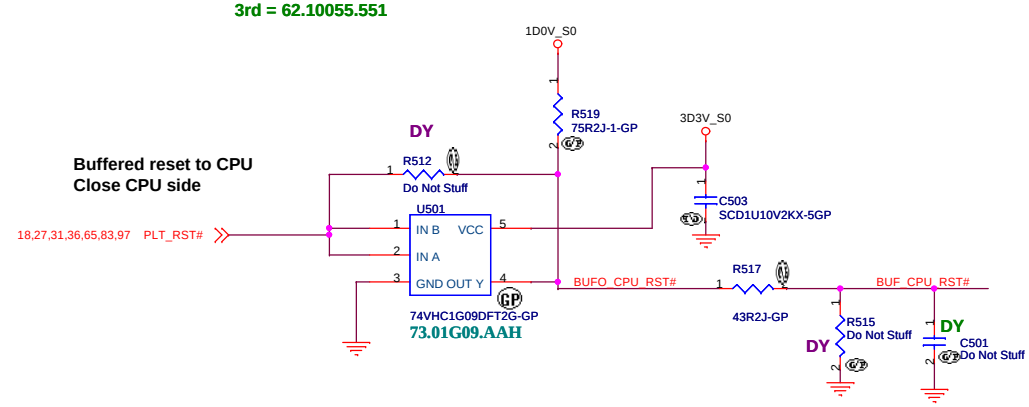
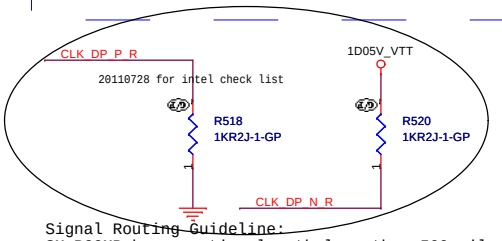
SSID = CPU

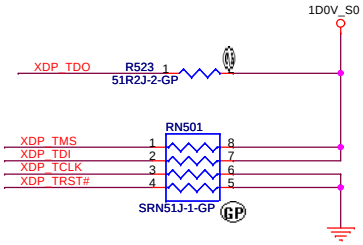


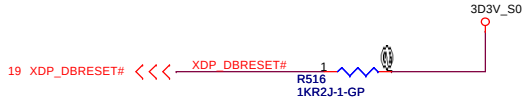


Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.



Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.





NOTE

	U501	R512	R519	R517	R515	C503	C501
HR	DY	0 ohm 63.R0034.1DL	DY	1.5K ohm 64.15015.6DL	750 ohm 64.75005.6DL	DY	DY
CRV	73.01G09.AAH	DY	75 ohm 63.75034.1DL	43 ohm 63.43034.1DL	DY	0.1uF 78.10423.2FL	DY

Default CRV

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Title	THERMAL/CLOCK/PM	
Size A3	Document Number LG4858L	Rev SB
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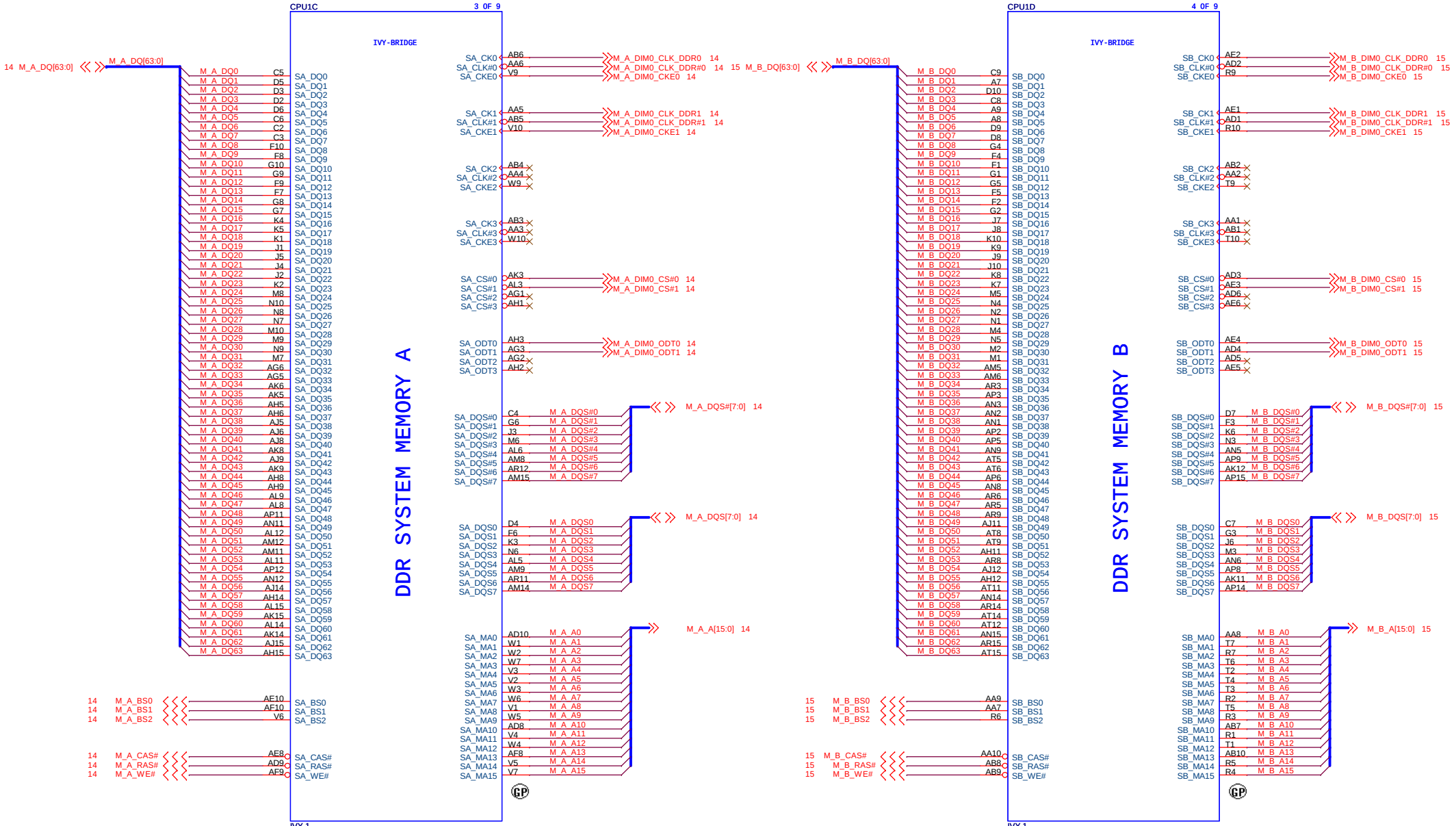
SSID = CPU



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Title	CPU (DDR)	
Size A3	Document Number LG4858L	Rev SB
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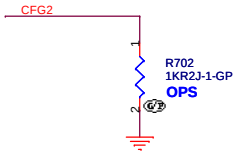
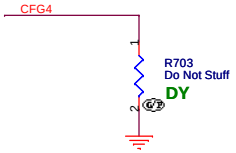
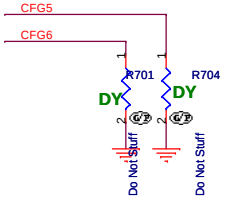
SSID = CPU



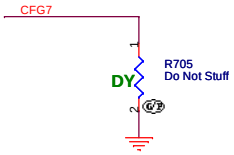
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



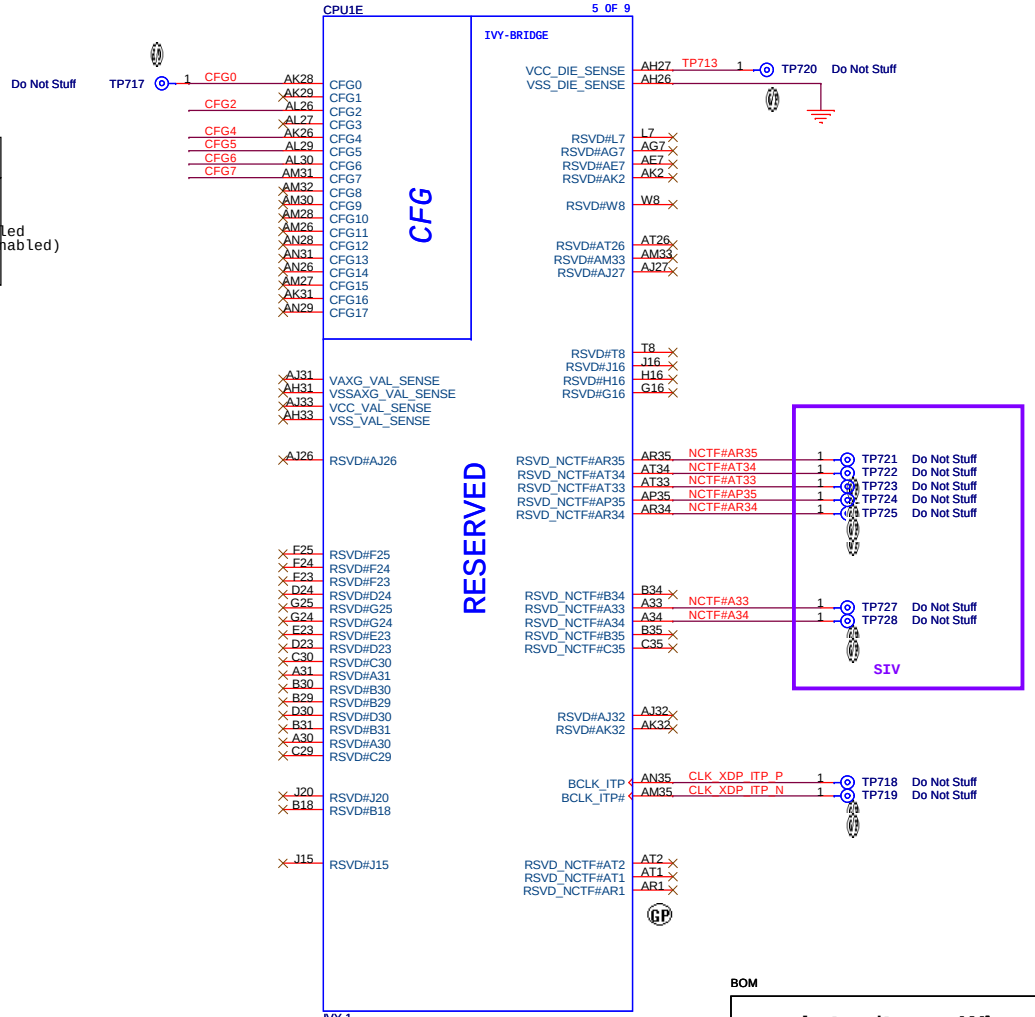
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



62.10040.821

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SSID = CPU

POWER

CPU1F

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IVY-BRIDGE

PEG AND DDR

SVID

SENSE LINES

CORE SUPPLY

VCC_CORE

VCC CORE:53A

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 Do Not Stuff
C804 Do Not Stuff
C811 SC10U6D3V5KX-1GP
DY DY

C817 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 Do Not Stuff
C833 Do Not Stuff
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP
DY DY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

BOM_CTRL

62.10040.821

VCCIO:8.5A

1D0V_S0

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 SC10U6D3V5KX-1GP

1D0V_S0

C812 C813 C814 C829 C830 C842 C843 C844 C845 SC10U6D3V5KX-1GP

-to 17pcs

TC8xx 470uF x2

R807 need to close to CPU

R807 75R2F-2-GP 110722 Ge 1D0V_S0

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK_R R805 Do Not Stuff H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT_R R806 Do Not Stuff H_CPU_SVIDDAT 42

R804 130R2F-1-GP 1D0V_S0

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D0V_S0

R808 10R2F-L-GP
VCCIO_SENSE
VSSIO_SENSE
R809 10R2F-L-GP

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 VCCIO_SENSE TP802 Do Not Stuff
VSS_SENSE_VCCIO A10 VSSIO_SENSE TP803 Do Not Stuff

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Title	mCPU (VCC_CORE)		
Size: Custom	Document Number: LG4858L		Rev: SB
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SSID = CPU

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

M3 - Processor Generated SO-DIMM VREF_DQ

M_VREF_DQ_DIMM0 — R915 1 — DY — Do Not Stuff
M_VREF_CA_DIMM0 — R916 1 — Do Not Stuff — DY
RN903 Do Not Stuff DY
12 DDR_WR_VREF01
12 DDR_WR_VREF02

POWER

CPU1G — 7 OF 9 — IVY-BRIDGE

VCC_GFXCORE

GRAPHICS: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17 — VAXG1 … VAXG54

C901 C902 C903 C904 C905 C906 — SC10U6D3V5KX-1GP — R-C901 Not Stuff DY
C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP — RC902 Not Stuff DY

SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37
SA_DIMM_VREFDQ — B4
SB_DIMM_VREFDQ — D1

DDR3 -1.5V RAILS

VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

PROCESSOR VDDQ: 12A

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP — SIV — 1D5V_S0
TC902 Do Not Stuff DY
TC9xx 330uF

SA RAIL

VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

PROCESSOR VCCSA: 6A

VCCSA — C916 C915 C917 — SC10U6D3V5KX-1GP
TC9xx 330uF

R902 need be close to pin H23.

MISC

VCCSA_SENSE — H23 — VCCSA_SENSE — VCCSA_SENSE 48
VCCSA_VID0 — C22 — VCCSA_SELECT0 48
VCCSA_VID1 — C24 — VCCSA_SELECT1 48
VCCIO_SEL — A19 — GP

1.8V RAIL

1D8V_S0 — **VCCPLL:1.5A**
C925 C923 C922 — SC10U6D3V5KX-1GP — SC1U10V2KX-1GP — C924 SC1U10V2KX-1GP
VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2
TC9xx 330uF

IVY-1

62.10040.821

BOM_CTRL
SIV
3D3V_S5 — R913 Do Not Stuff DY — H_VCCIO_SEL
ES2 dummy R913

1D0V_S0 — R917 Do Not Stuff DY — VCCSA_SELECT0 — R918 1KR2J-1-GP
1D0V_S0 — R920 Do Not Stuff DY — VCCSA_SELECT1 — R919 1KR2J-1-GP
SIT

Close to CPU
VCC_GFXCORE — R906 100R2F-L1-GP-U — VCC_AXG_SENSE — VSS_AXG_SENSE — R907 100R2F-L1-GP-U
SIV for intel recommend

NOTE

	R906/R907
HR	100 ohm 64.10005.6DL
CRV	10 ohm 64.10R05.6DL

Default CRV

BOM

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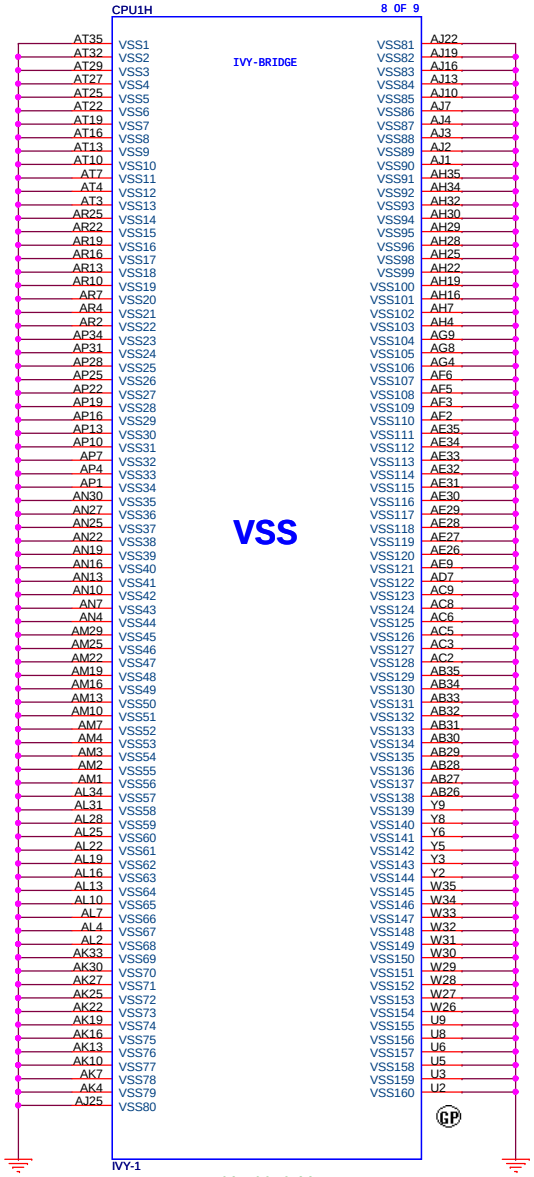
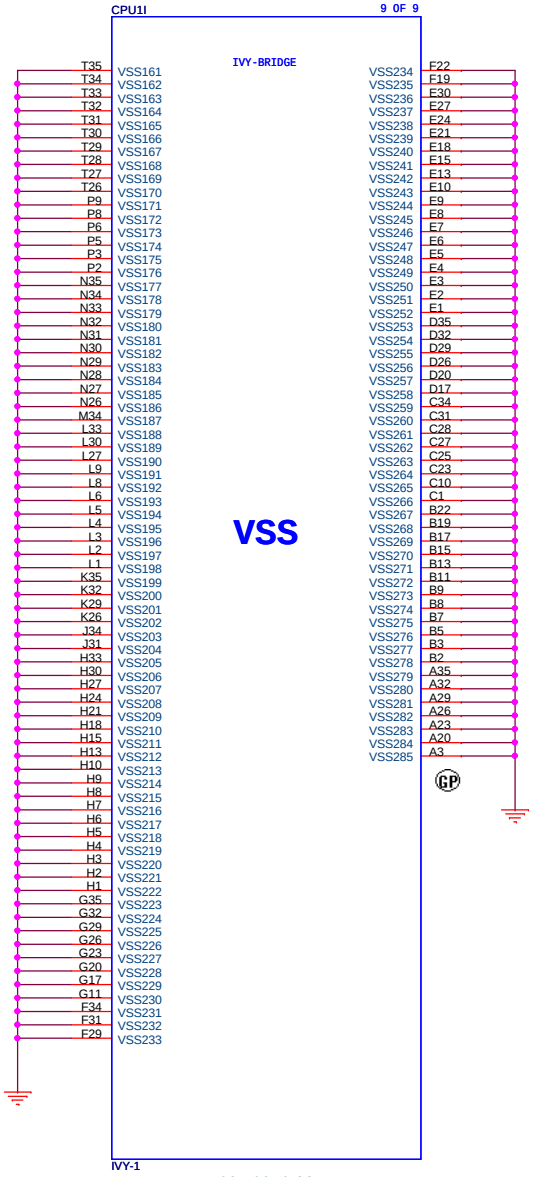
Title: ***mCPU (VCC_GFXCORE)***
Size: A3 | Document Number: **LG4858L** | Rev: SB
Date: Friday, March 16, 2012 | Sheet 9 of 103

SSID = CPU



62.10040.821

BOM_CTRL



62.10040.821

BOM_CTRL

BOM

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Title	*CPU(VSS)*	
Size A3	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 10 of 103	

(Reserved)

BOM

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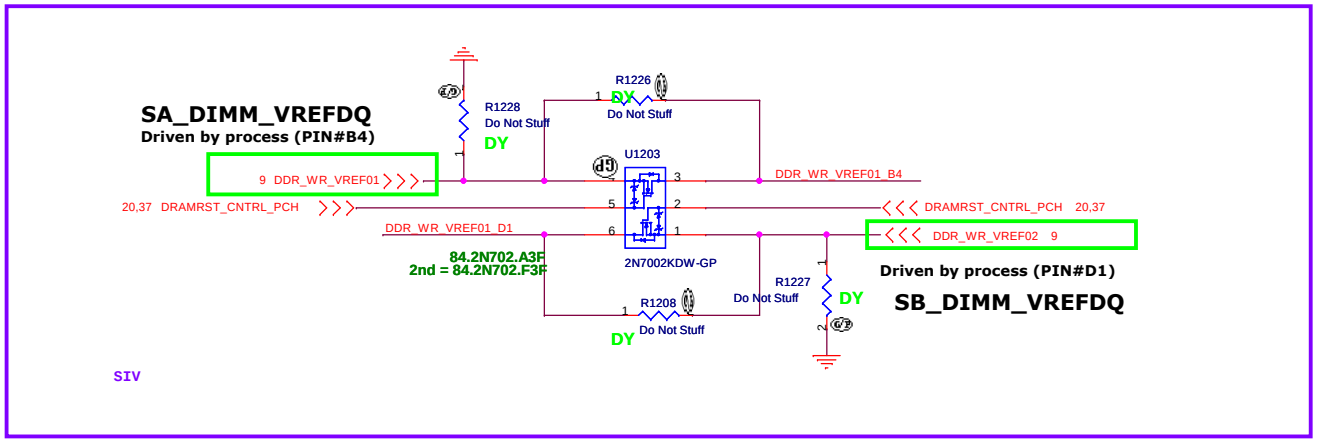
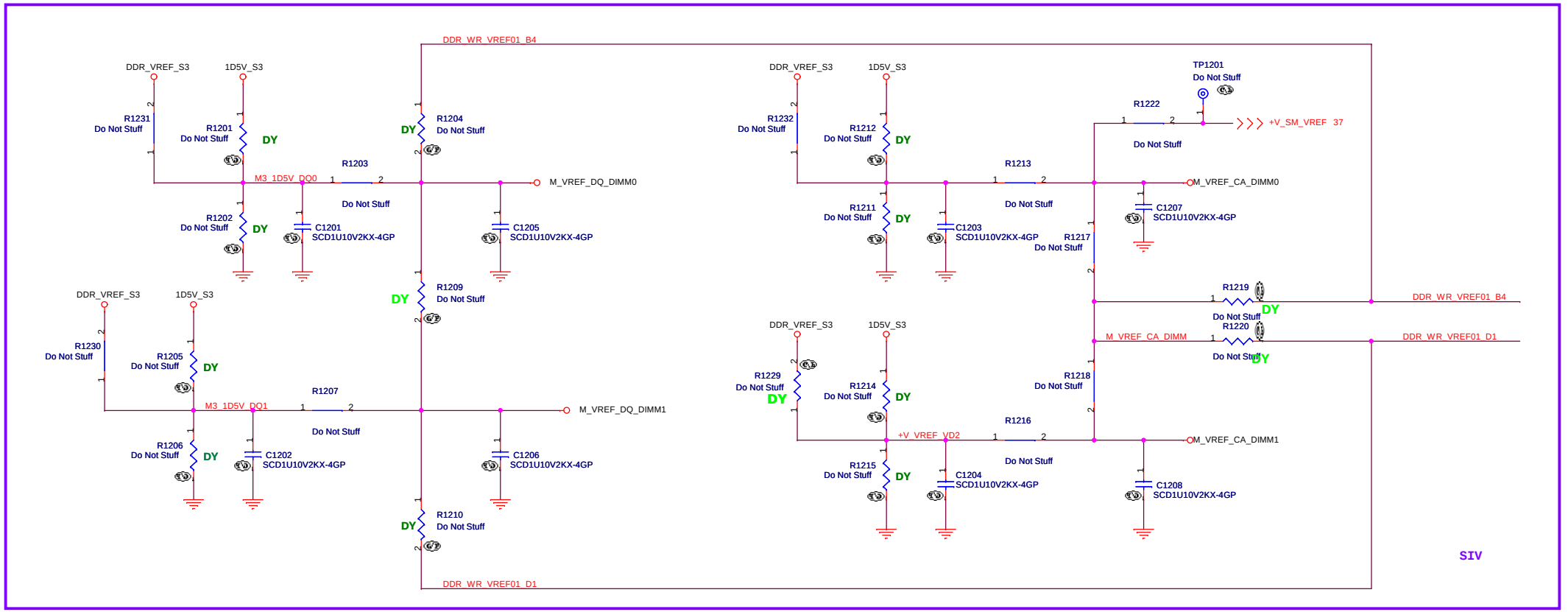
Title	***XDP***		
Size	Document Number **LG4858L**		Rev **SB**
Date: Friday, March 16, 2012		Sheet 11 of 103	

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

For CRV:





BOM

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Title	*M1 & M3 Implementation*	
Size	Document Number **LG4858L**	Rev **SB**
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SSID = MEMORY

DIMM1

DDR3-240P-28-GP

M_A_A[15:0] 6

M_A_BS2 6

M_A_BS0 6

M_A_BS1 6

M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6

M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6

M_A_DIM0_ODT1 6

M_VREF_CA_DIMM0

M_VREF_DQ_DIMM0

DDR3_DRAMRST# 15,37

M_A_RAS# 6

M_A_WE# 6

M_A_CAS# 6

M_A_DIM0_CS#0 6

M_A_DIM0_CS#1 6

M_A_DIM0_CKE0 6

M_A_DIM0_CKE1 6

M_A_DIM0_CLK_DDR0 6

M_A_DIM0_CLK_DDR#0 6

M_A_DIM0_CLK_DDR1 6

M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 15,20,65,69

PCH_SMBCLK 15,20,65,69

TS#_DIMM0_1 15

SA0_DIM0

SA1_DIM0

0D75V_S0

3D3V_S0

1D5V_S3

VTT1

VTT2

RESET#

VREF_CA

VREF_DQ

ODT0

ODT1

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

RN1401
SRN10KJ-5-GP
SIV

Thermal EVENT
R1403 10KR2J-3-GP

C1401 SCD1U10V2KX-5GP
C1402 Do Not Stuff
DY

SODIMM A DECOUPLING

TC1401 SE390U2D5VM-12-GP
77.53971.01L
SIT

C1403 SC1U06D3V5KX-1GP
C1404 SC1U06D3V5KX-1GP
C1405 Do Not Stuff
C1406 SC1U06D3V5KX-1GP
C1407 SC1U06D3V5KX-1GP
C1408 Do Not Stuff
C1409 Do Not Stuff
C1410 Do Not Stuff
DY

C1414 SCD1U10V2KX-5GP
C1415 SCD1U10V2KX-5GP
C1416 SCD1U10V2KX-5GP
C1417 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

C1418 Do Not Stuff
C1419 SC1U06D3V2KX-GP
C1420 Do Not Stuff
C1421 SC1U06D3V2KX-GP
C1422 Do Not Stuff
DY

FC1402 Do Not Stuff
SIV

62.10017.R91

1st = 62.10017.V61

2nd = 62.10017.X51

BOM_CTRL

BOM

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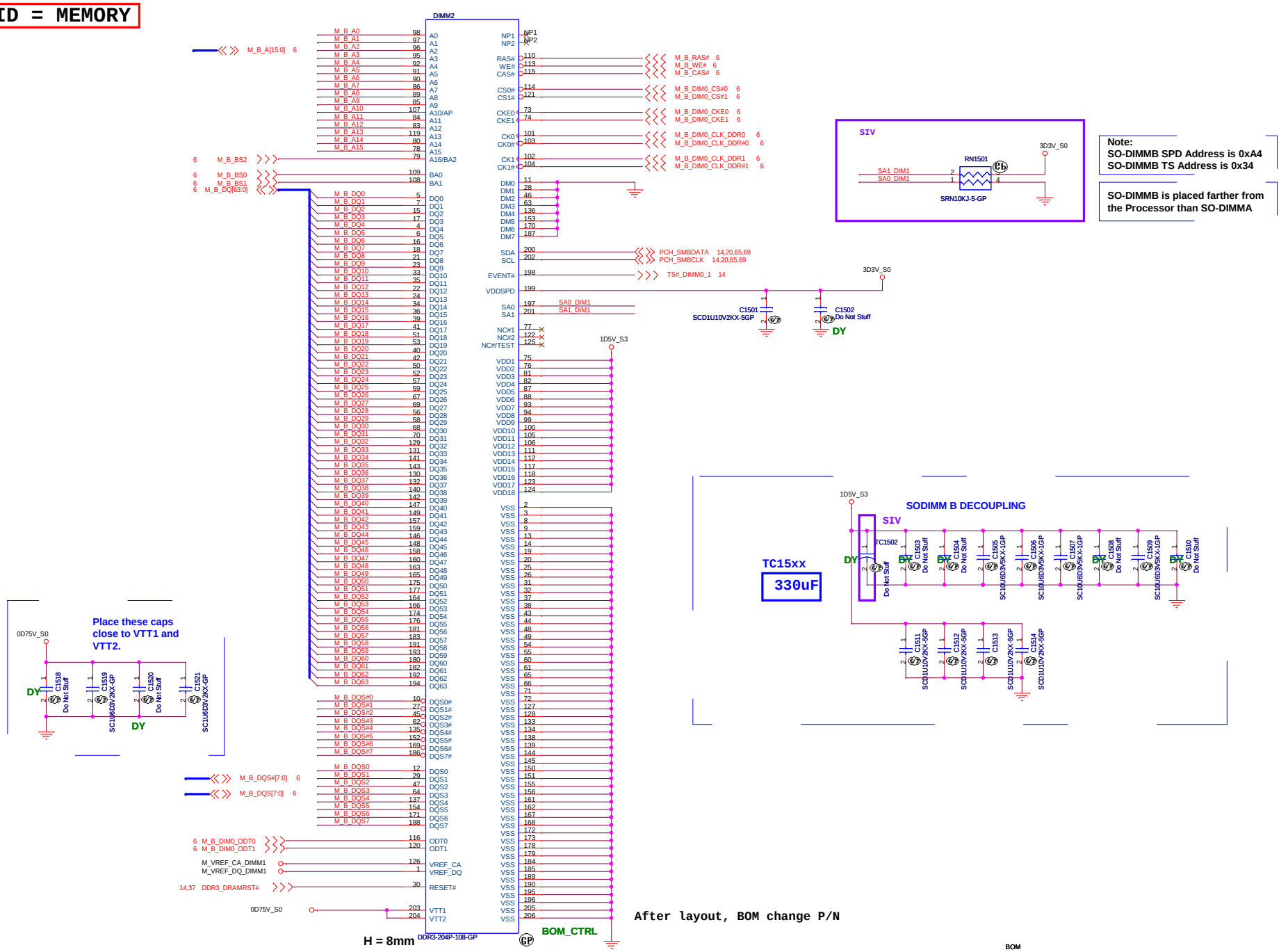
Title: ***DDR3-SODIMM1***

Size | Document Number: **LG4858L** | Rev: **SB**

Date: Friday, March 16, 2012 | Sheet 14 of 103

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

H = 8mm

62.10017.X41

1st = 62.10024.G21

2nd = 62.10017.X41

After layout, BOM change P/N

BOM

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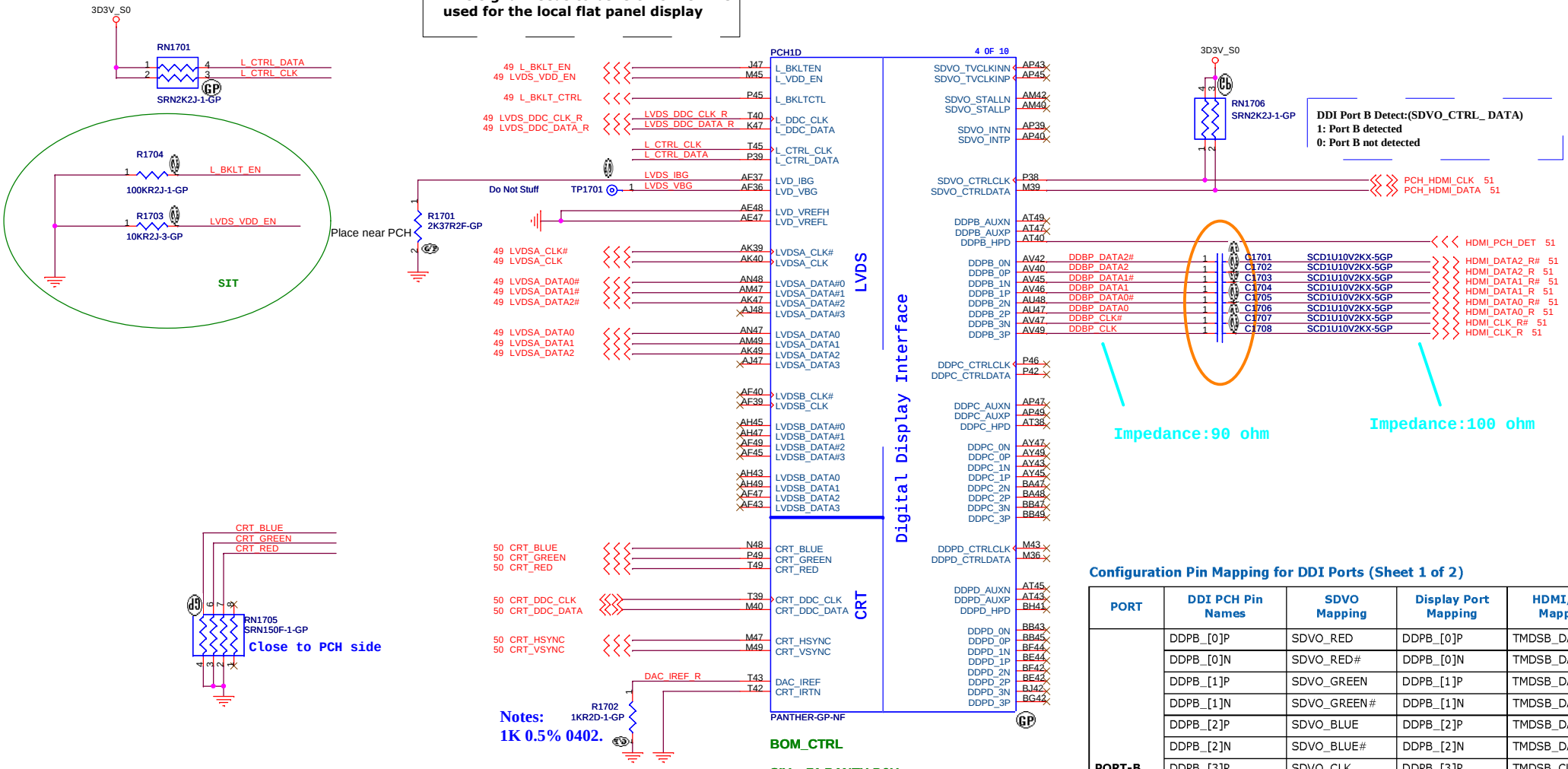
Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
	LG4858L	SB

Date: Friday, March 16, 2012 Sheet 15 of 103

L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display



Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

BOM

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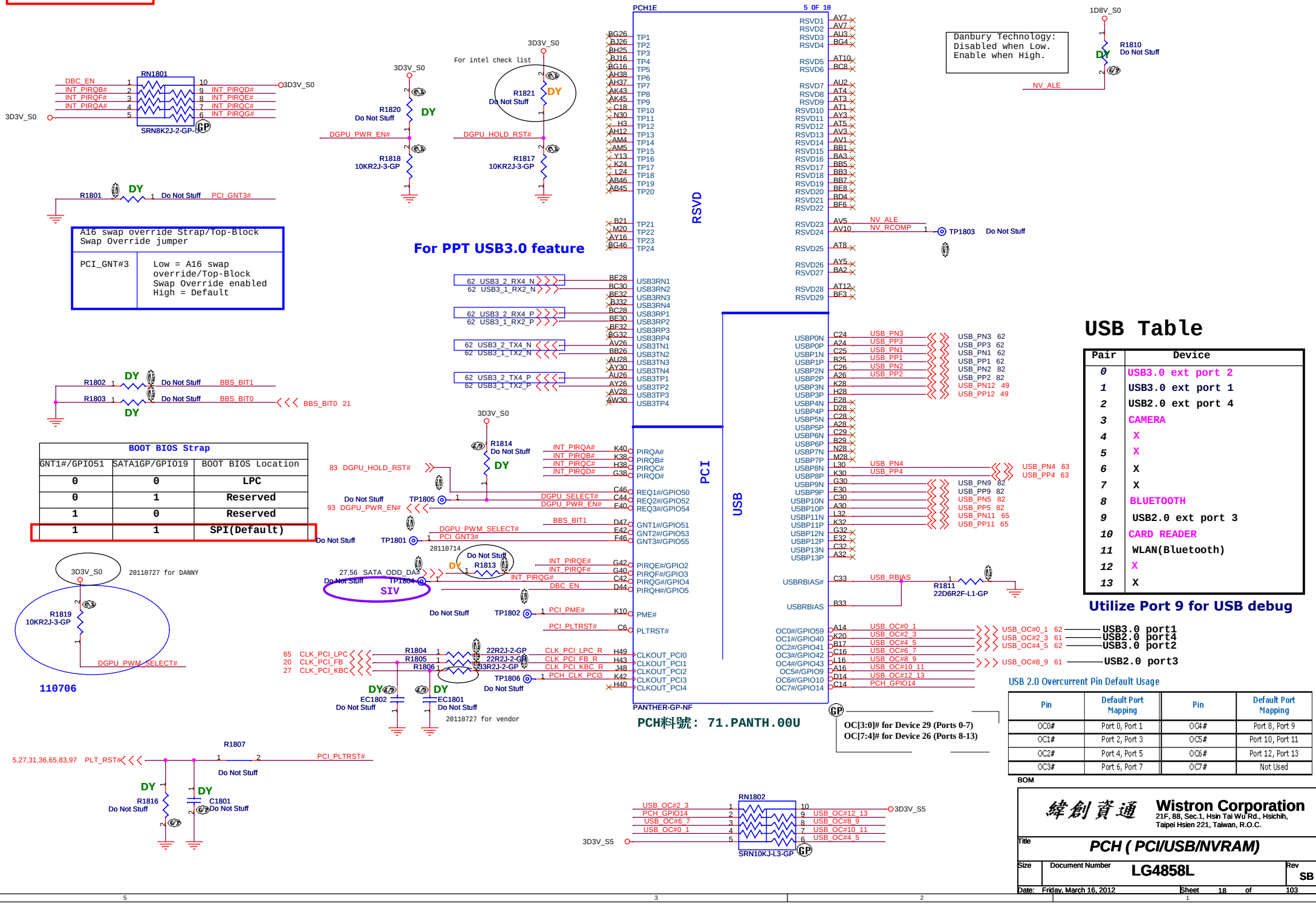
Title: PCH (LVDS/CRT/HDMI)

Size | Document Number: LG4858L | Rev: SB

Date: Friday, March 16, 2012 | Sheet 17 of 103

SSID = PCH


PCH1E
5 OF 10
RSVD
PCI
USB
PANTHER-GP-NF
For PPT USB3.0 feature
Danbury Technology:
Disabled when Low.
Enable when High.
A16 swap override Strap/Top-Block
Swap Override jumper
PCI_GNT3# Low = A16 swap override/Top-Block Swap Override enabled High = Default
BOOT BIOS Strap
GNT1#/GPIO51 SATA1GP/GPIO19 BOOT BIOS Location
0 0 LPC
0 1 Reserved
1 0 Reserved
1 1 SPI(Default)
SIV
110706
20110727 for DANNY
20110727 for vendor
PCH料號: 71.PANTH.00U
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)
USB Table
Pair Device
0 USB3.0 ext port 2
1 USB3.0 ext port 1
2 USB2.0 ext port 4
3 CAMERA
4 X
5 X
6 X
7 X
8 BLUETOOTH
9 USB2.0 ext port 3
10 CARD READER
11 WLAN(Bluetooth)
12 X
13 X
Utilize Port 9 for USB debug
USB3.0 port1
USB2.0 port4
USB3.0 port2
USB2.0 port3
USB 2.0 Overcurrent Pin Default Usage
Pin Default Port Mapping Pin Default Port Mapping
OC0# Port 0, Port 1 OC4# Port 8, Port 9
OC1# Port 2, Port 3 OC5# Port 10, Port 11
OC2# Port 4, Port 5 OC6# Port 12, Port 13
OC3# Port 6, Port 7 OC7# Not Used
BOM
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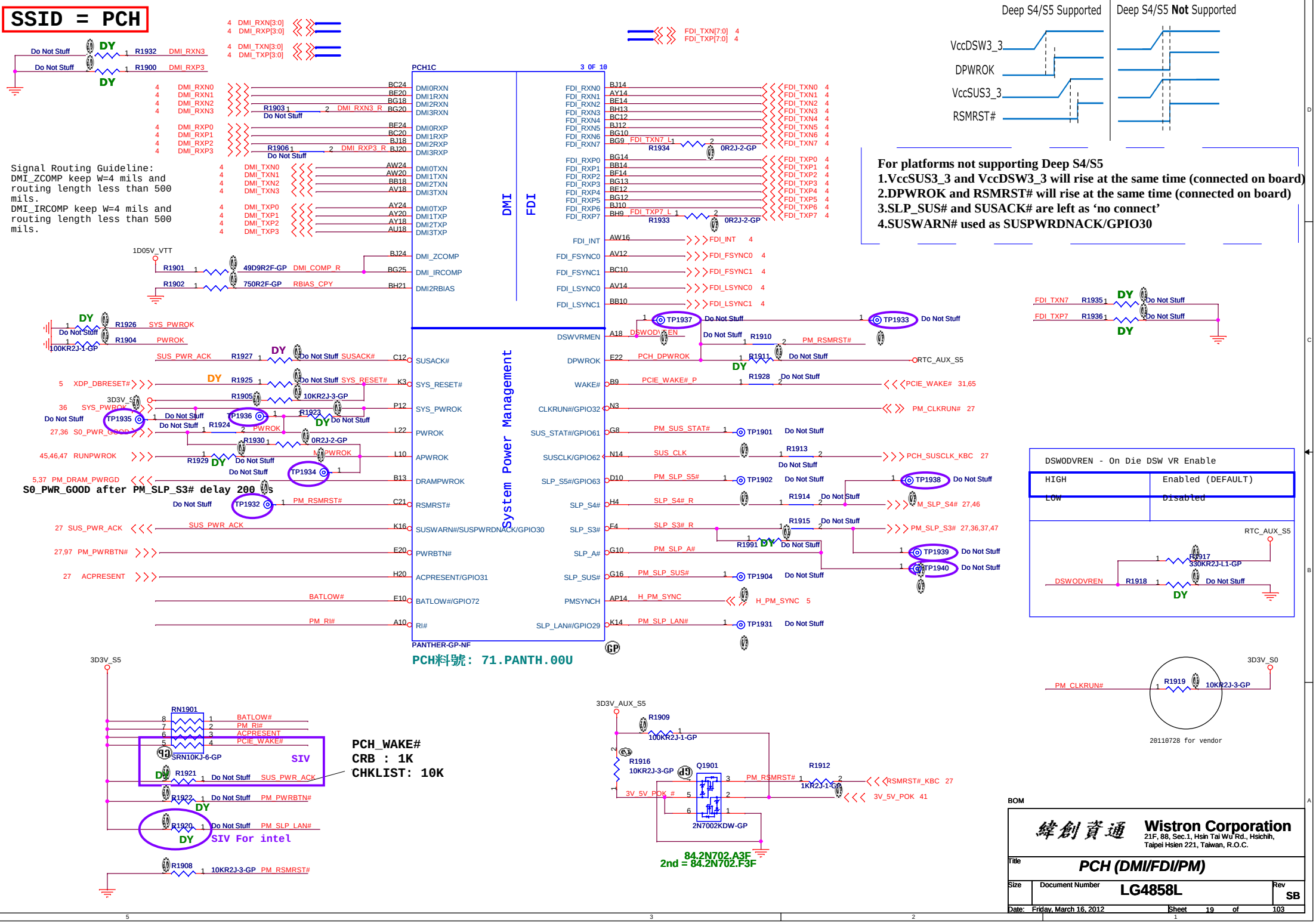
Title PCH (PCI/USB/NVRAM)
Size Document Number LG4858L Rev SB
Date: Friday, March 16, 2012 Sheet 18 of 103

SSID = PCH


Deep S4/S5 Supported
Deep S4/S5 Not Supported
VccDSW3_3
DPWROK
VccSUS3_3
RSMRST#
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.
PCH1C
3 OF 10
DMI
FDI
System Power Management
PANTHER-GP-NF
PCH料號: 71.PANTH.00U
S0_PWR_GOOD after PM_SLP_S3# delay 200 us
PCH_WAKE#
CRB : 1K
CHKLIST: 10K
SIV
SIV For intel
84.2N702.A3F
2nd = 84.2N702.F3F
DSWODVREN - On Die DSW VR Enable
HIGH Enabled (DEFAULT)
LOW Disabled
20110728 for vendor
Wistron Corporation
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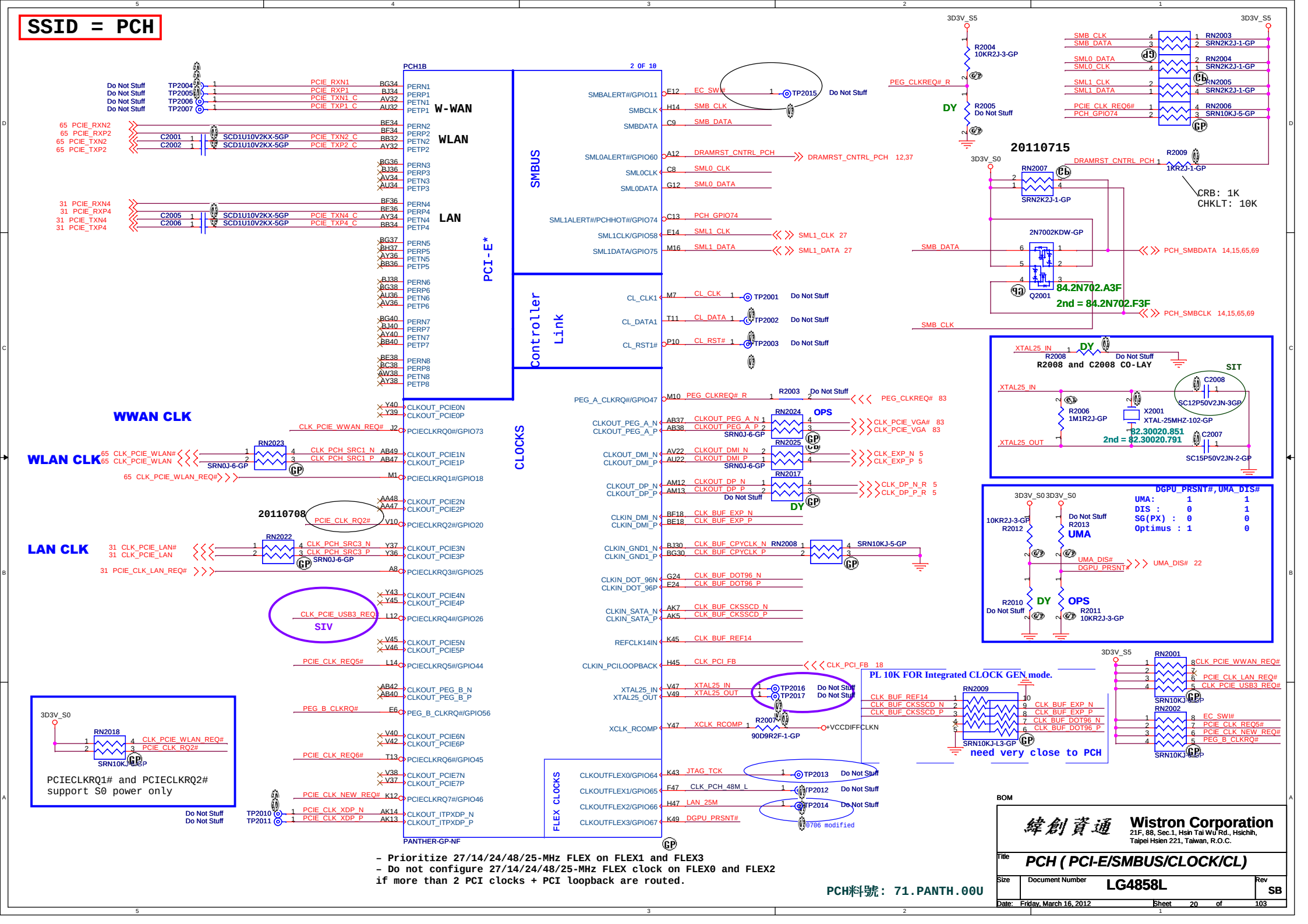
Taipei Hsien 221, Taiwan, R.O.C.
PCH (DMI/FDI/PM)
LG4858L
Rev SB
Date: Friday, March 16, 2012
Sheet 19 of 103

SSID = PCH



BOM

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Title	PCH (PCI-E/SMBUS/CLOCK/CL)		
Size	Document Number	LG4858L	Rev SB
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SSID = PCH

NOTE

	R2111,R2118~R2120,R2125
HR	0 ohm 63.R0034.1DL
CRV	22 ohm 64.22R05.6DL

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

PCH1A — 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
SATA: SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATA3RCOMPO, SATA3COMPI, SATA3RBIAS, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
SATA 6G

PANTHER-GP-NF

PCH料號: 71.PANTH.00U

RTC_AUX_S5 Do Not Stuff — RN2104 SRN20KJ-1-GP — TP2111 — C2103 SC1U6D3V2KX-GP — SIT

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2 — X2101 — C2101 SC6P50V2CN-1GP — C2102 SC6P50V2CN-1GP — X-32D768KHZ-34GPU — SIT

Q2130 2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.W31

D2130 Do Not Stuff — R2130 0R2J-2-GP — R2131 Do Not Stuff — DY

KBC_RTCRST# — 27 RTCRST_ON — KBC_RTCRST# 27

TP2114 Do Not Stuff — RTC_X1
TP2115 Do Not Stuff — RTC_X2
TP2112 Do Not Stuff — RTC_RST#
G2101 Do Not Stuff — C2104 — SRTC_RST#
R2104 1M1R2J-GP — SM_INTRUDER#
R2105 330KR2F-L-GP — PCH_INTVRMEN
RTC_AUX_S5 — TP2113 Do Not Stuff

HDA_BITCLK — HDA_SYNC — 29 HDA_SPKR — HDA_RST# — 29 HDA_SDIN0

29 HDA_CODEC_SDOUT — R2123 33R2J-2-GP — HDA_SDOUT
29 HDA_CODEC_RST# — RN2102 SRN33J-5-GP — HDA_RST#
29 HDA_CODEC_BITCLK — HDA_BITCLK_C — ER2233 Do Not Stuff — HDA_BITCLK For EMC

Flash Descriptor Security Overide

HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO — R2102 Do Not Stuff — HDA_SDOUT — DY

27 ME_UNLOCK — R2107 1KR2J-1-GP — HDA_SDOUT — Do Not Stuff — TP2105 — PCH_GPIO33

NO REBOOT STRAP

3D3V_S0 — R2106 Do Not Stuff — HDA_SPKR — DY

No Reboot Strap

HDA_SPKR	Low = Default High = No Reboot

Do Not Stuff — TP2106 — 4K7R2J-2-GP R2121 — PCH_JTAG_TCK_BUF
Do Not Stuff — TP2102 — PCH_JTAG_TMS
Do Not Stuff — TP2103 — PCH_JTAG_TDI
Do Not Stuff — TP2104 — PCH_JTAG_TDO

+3VS_+1.5VS_HDA_IO — R2103 1KR2J-1-GP — HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V (Default) High = 1.5V

27,60,65 SPI_CLK_R — R2108 33R2J-2-GP — PCH_SPI_CLK
27,60,65 SPI_CS0#_R — R2109 33R2J-2-GP — PCH_SPI_CS0# — SIT
27,60,65 SPI_SI_R — R2110 33R2J-2-GP — PCH_SPI_SI
27,60,65 SPI_SO_R

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

Do Not Stuff — R2122 — DY
84.2N702.J31
2ND = 84.2N702.W31
Q2101 2N7002K-2-GP
HDA_SYNC — HDA_CODEC_SYNC_L — R2124 33R2J-2-GP — HDA_CODEC_SYNC 29
R2127 1MR2F-GP
5V_S0

HDA_CODEC_BITCLK — EC2102 DY Do Not Stuff
HDA_CODEC_SDOUT — EC2103 DY Do Not Stuff
SPI_CS0#_R — EC2101 DY Do Not Stuff

22 ohm 5%
C38 LPC_AD0_TPM R2111 — 22R2J-2-GP — LPC_AD0
A38 LPC_AD1_TPM R2118 — 22R2J-2-GP — LPC_AD1
B37 LPC_AD2_TPM R2119 — 22R2J-2-GP — LPC_AD2
C37 LPC_AD3_TPM R2120 — 22R2J-2-GP — LPC_AD3
LPC_AD[0..3] — LPC_AD[0..3] 27,65
D36 LPC_FRAME# — R2125 22R2J-2-GP — LPC_FRAME# 27,65
E36 GPIO23
K36
V5 — INT_SERIRQ 27

HM70

AM3 SATA0RXN — AM1 SATA0RXP — AP7 SATA_TXN1_C C2105 — AP5 SATA_TXP1_C C2106 — SCD01U16V2KX-3GP — SATA_RXN1_C 56 — SATA_RXP1_C 56 — SATA_TXN1 56 — SATA_TXP1 56
SATA0TXN — SATA0TXP
AM10 SATA1RXN — AM8 SATA1RXP — AP11 SATA1TXN — AP10 SATA1TXP

HDD1

HM70 SATA port 1 and port3 disable

AD7 SATA2RXN — AD5 SATA2RXP — AH5 SATA2TXN — AH4 SATA2TXP
AB8 SATA3RXN — AB10 SATA3RXP — AF3 SATA3TXN — AF1 SATA3TXP

Move Cap close to Device or Connector.

Y7 SATA4RXN — Y5 SATA4RXP — AD3 SATA4TXN — AD1 SATA4TXP — SATA_RXN4_C 56 — SATA_RXP4_C 56 — SATA_TXN4_C C2109 — SATA_TXP4_C C2110 — SCD01U16V2KX-3GP — SATA_TXN4_C 56 — SATA_TXP4_C 56 — SATA_TXN4 56 — SATA_TXP4 56

ODD

Y3 SATA5RXN — Y1 SATA5RXP — AB3 SATA5TXN — AB1 SATA5TXP — SATA_RXN5 — SATA_RXP5 — SATA_TXN5 — SATA_TXP5 — TP2107 Do Not Stuff — TP2108 Do Not Stuff — TP2109 Do Not Stuff — TP2110 Do Not Stuff

Delete ESATA

Y11 SATAICOMPO — Y10 SATAICOMPI — SATA_COMP — R2112 37D4R2F-GP — 1D05V_VTT
AB12 SATA3RCOMPO — AB13 SATA3COMPI — SATA3_COMP — R2113 49D9R2F-GP — 1D05V_VTT
AH1 SATA3RBIAS — RBIAS_SATA3 — R2114 750R2F-GP For Ge

LA37/LA57/CRV-Std:750ohm
LA47: 806 ohm

P3 SATALED# — SATA_LED# — TP2130 Do Not Stuff
V14 SATA0GP/GPIO21 — GPIO21_SATA_DET#0 — R2232 Do Not Stuff — SATA_DET#0
P1 SATA1GP/GPIO19 — GPIO19_BBS_BIT0 — R2231 Do Not Stuff — BBS_BIT0 18

3D3V_S0
SATA_DET#0 — R2129 10KR2J-3-GP
20110727 for vendor — INT_SERIRQ — RN2101 SRN10KJ-5-GP
22 — PSW_CLR# — SIV
GPIO23 — R2128 10KR2J-3-GP

BOM

110706 modified

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number: LG4858L		Rev: SB
Date: Friday, March 16, 2012	Sheet 21 of 103		

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

LOW: ODD exist
HIGH: ODD non-exist

PCH_GPIO15 pull high => 11252 or 11291
PCH_GPIO15 pull Low => 11326 or 12206

Note

	R2202	----
HR	200K ohm 64.20035.6DL	
CRB	10K ohm 63.10334.1DL	

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PCH料號: 71.PANTH.00U

BOM

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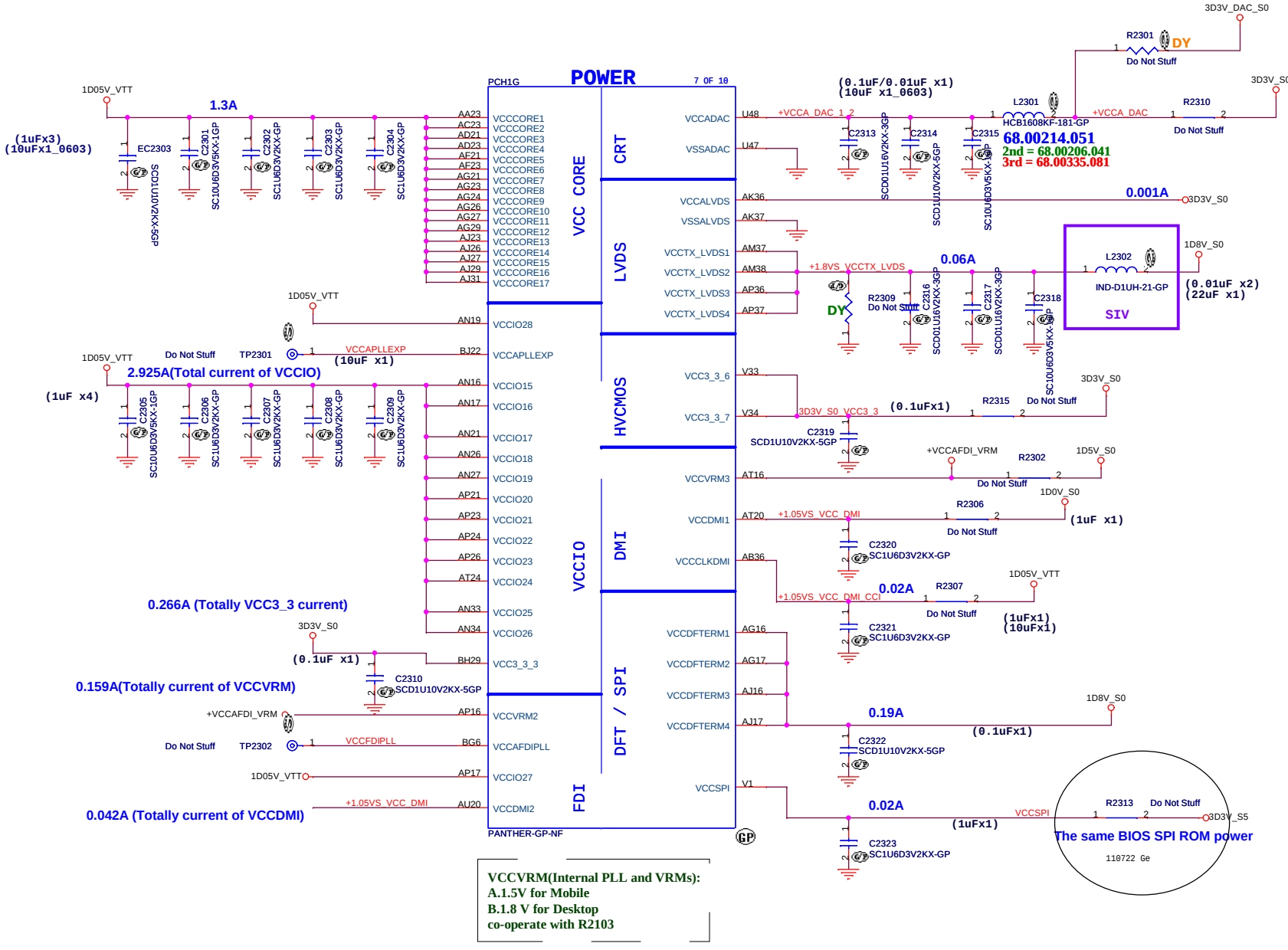
Title: PCH (GPIO/CPU)
Size: Document Number: LG4858L Rev: SB
Date: Friday, March 16, 2012 Sheet 22 of 103

SSID = PCH 6A



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture

VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

BOM

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Title	PCH (POWER1)	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 23 of 103	

SSID = PCH

POWER

PCH1J

10 OF 10

after layout, place 4.7uF *3

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM)

0.097A (Totally current of VCCSUS3_3)

0.001A

0.002A

0.08A

0.055A

0.095A

0.001A

0.01A

6uA

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

PANTHER-GP-NF

BOM

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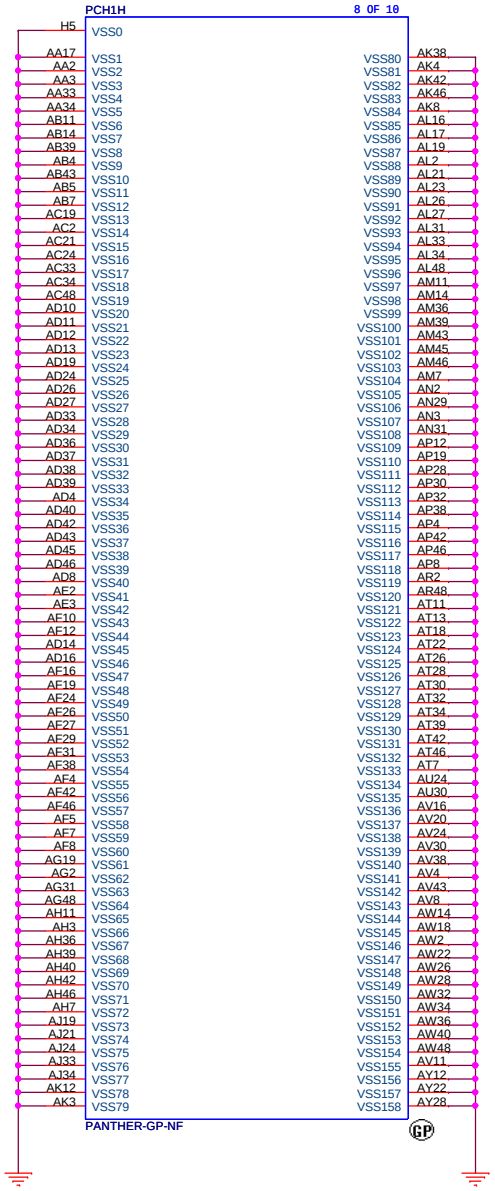
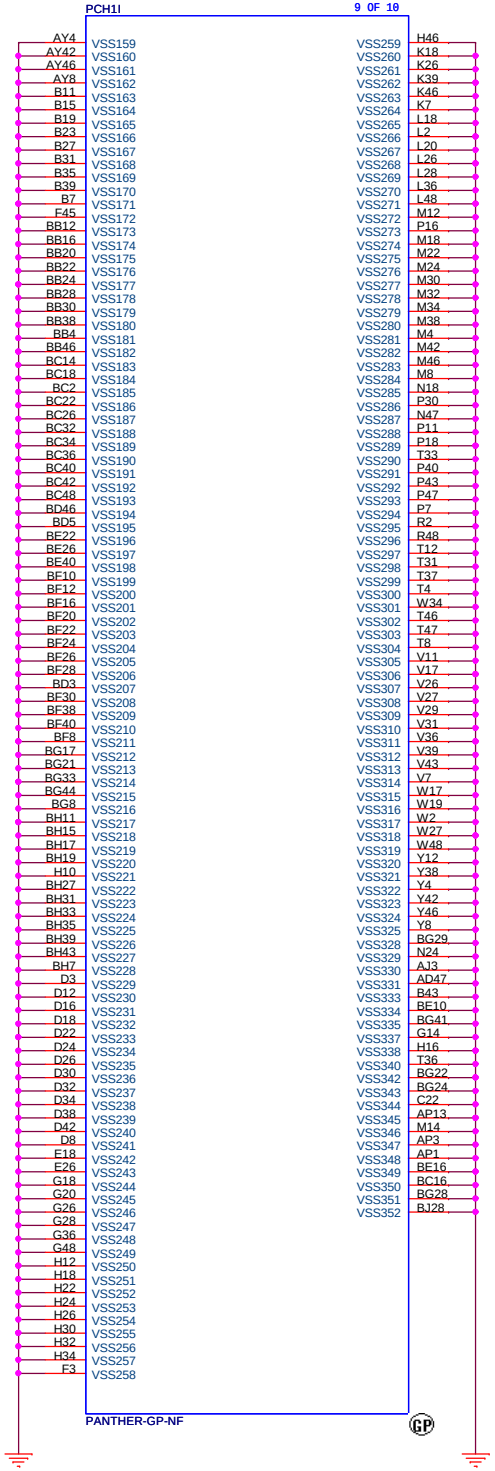
Title	PCH (POWER2)	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 24 of 103	

SSID = PCH





BOM

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Title	PCH (VSS)	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 25 of 103	

SSID = KBC

If use PSL function, please connect to 3D3V_AUX_S5
If no use PSL function, please connect 3D3V_AUX_KBC

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

65W_90W#
High: 65W / Low 90W

NOTE:
Locate resistors R2719 and R2722 close to the NPCE885P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

71.00885.A0G

R2701 and C2716 Need very close to EC

<------ TP
<------ BATTERY / CHARGER
<------PCH / eDP

EC_GPIO47 High Active

84.2N702.J31
2nd = 84.2N702.W31

83.00016.K11
2ND = 83.00016.F11

Prevent BIOS data loss solution

84.T3906.A11
2nd = 84.03906.F11

EC GPIO standard PH/PL

LILI Multi GPIO setting

84.DMN66.03F
2ND = 84.2N702.A3F

64.47025.6DL

MODEL_ID_AD (Pin100)	Pull-Low Register	Pull-High Register	Voltage	
LG48 UMA	100.0 K	10.0 K	3.000 V	64.10025.6DL
LG48 OPTIMUS	100.0 K	20.0 K	2.750 V	64.20025.6DL
LG58 UMA	100.0 K	33.0 K	2.481 V	64.33025.6DL
LG58 OPTIMUS	100.0 K	47.0 K	2.245 V	64.47025.6DL

BOM

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Title: KBC Nuvoton NPCE795
Size: Document Number: LG4858L Rev: SB
Date: Friday, March 16, 2012 Sheet 27 of 103

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA 0905 change to 390p

3

Q6
MMBT3904WT1G-GP

C183
SC390P50V2KX-GP

2200p close to smsc2103 chip

2

DY

Q42
Do Not Stuff

C434
Do Not Stuff
DY

REMOTE2-

C569
SC2200P50V2KX-2GP

REMOTE2+

between CPU, VGA and DIMM on bottom side

T8

1

Q9
MMBT3904WT1G-GP

2200p close to smsc2103 chip

H_THERMDA

C389
SC2200P50V2KX-2GP

H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

T8= 86 degree

3D3V_S0

R2803
6K8R2J-GP

THERM_SYS_SHDN#

3D3V_S0

R2802
15KR2J-1-GP

THERM_SCI#

3D3V_S0

R260
68R2-GP

C388 SCD1U10V2KX-4GP

2103_VDD

U2801

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-

VDD
DP1
DN1
DP2/DN3
DN2/DP3

SMCLK
SMDATA
ALERT#
SYS_SHDN#
GND

SMBC_THERM 27,86
SMBD_THERM 27,86

THERM_SCI#
THERM_SYS_SHDN#

R272 Do Not Stuff

THERM_SCI#

EMC1423-1-AIZL-TR-GP

4 WIRE PWM Fan Control circuit

Close to connector

5V_S0

D2801
Do Not Stuff
Do Not Stuff
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
DY

C39
SC47U6D3VKX-GP

R426
10KR2J-3-GP

R2801
Do Not Stuff

R427
SIT
Do Not Stuff

FAN1

27 FAN_PWM

FAN_PWM

FAN_PWM_C

27 FAN_TACH

FAN_TACH

5V_S0_FAN

EC2801
SC470P50V2JN-GP

SIT

EC2802
SC470P50V2JN-GP

ACES-CON4-GP-U1

20.F0714.004
2nd = 20.D0196.104

TP2803
TP2802
TP2801
AFTP2804

FAN_PWM_C
FAN_TACH
5V_S0_FAN

3D3V_AUX_S5

D2803
Do Not Stuff
Do Not Stuff
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
DY

27,36,86 PURE_HW_SHUTDOWN#

DY
R2812
Do Not Stuff

DY
C2811
Do Not Stuff

Q2802

THERM_SYS_SHDN#

IMVP_PWRGD_T

2N7002K-2-GP

84.2N702.J31
2ND = 84.2N702.W31

3D3V_S0

DY
R2809
Do Not Stuff

SIV

3D3V_S0

R2810
Do Not Stuff

DY
R2811
Do Not Stuff

BOM

3D3V_S0

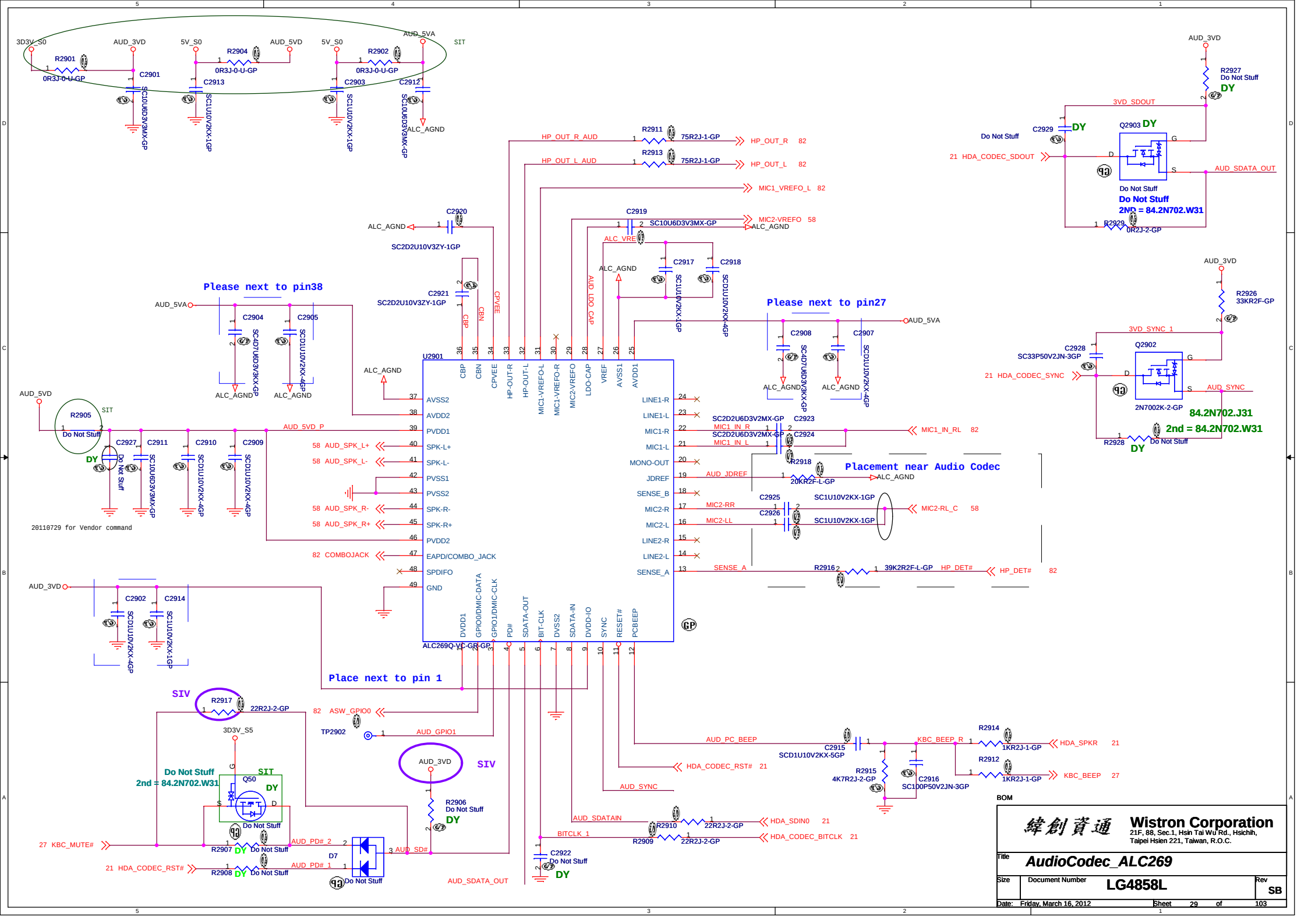
SIT

R2814
10KR2J-3-GP

IMVP_PWRGD 36,42

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

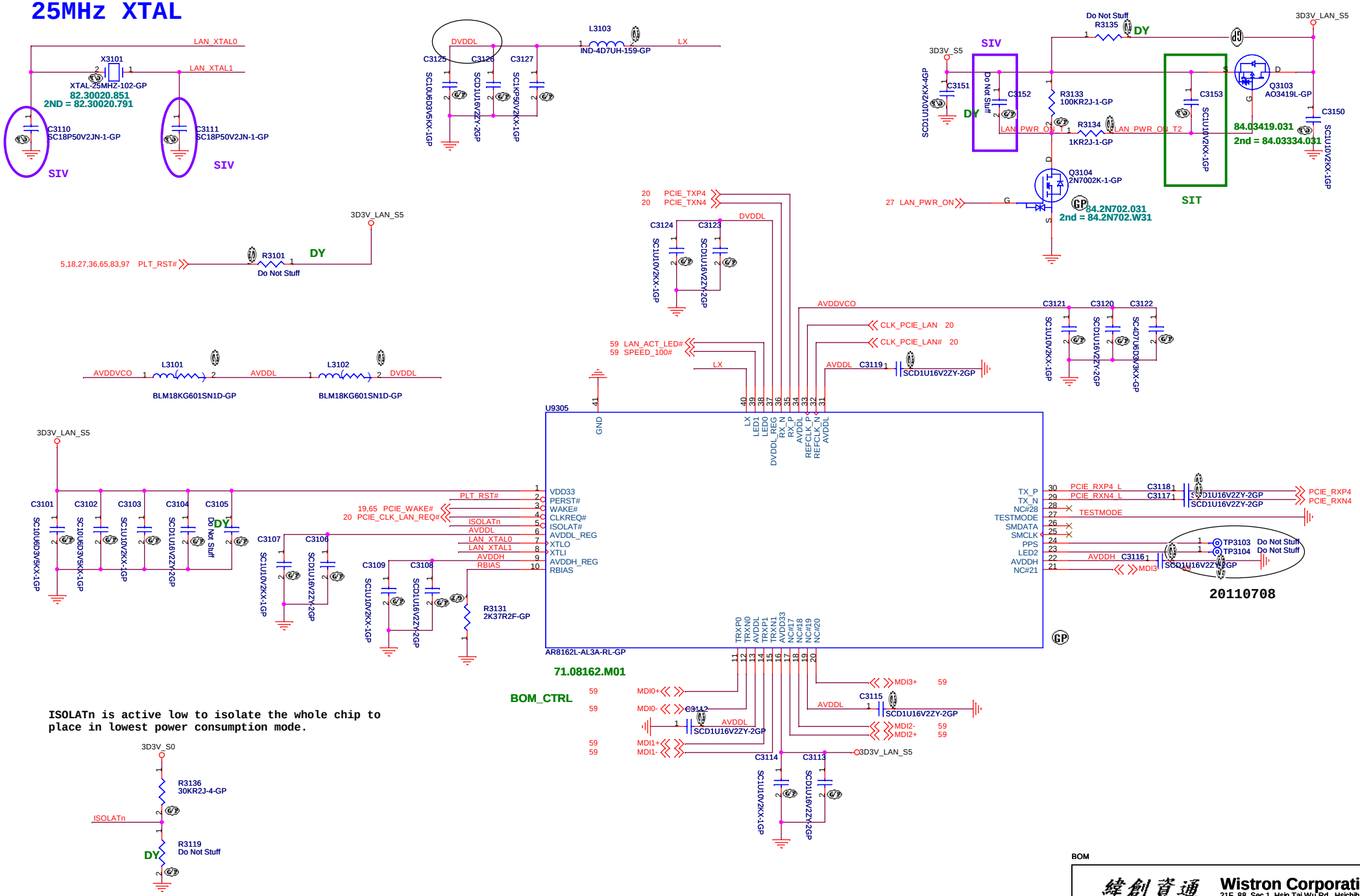
Title	THERMAL EMC1423	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 28 of 103	



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AudioCodec_ALC269***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 29 of 103	

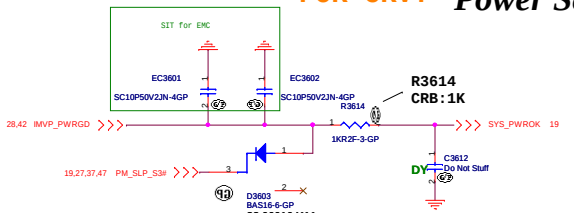
25MHz XTAL



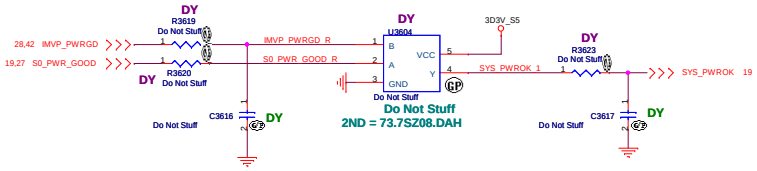
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LOM***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 31 of 103	

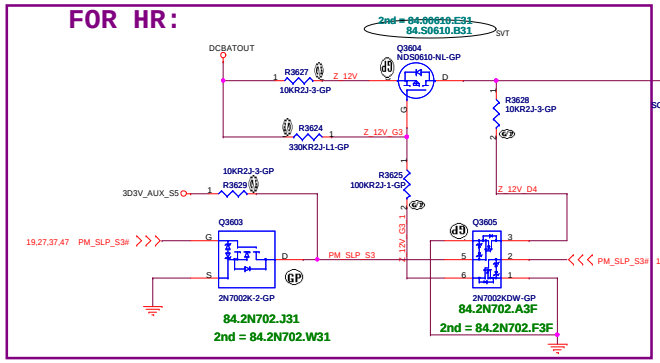
FOR CRV: Power Sequence

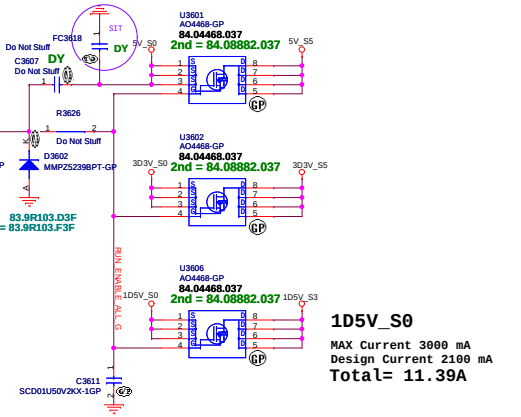


FOR HR:



FOR HR:

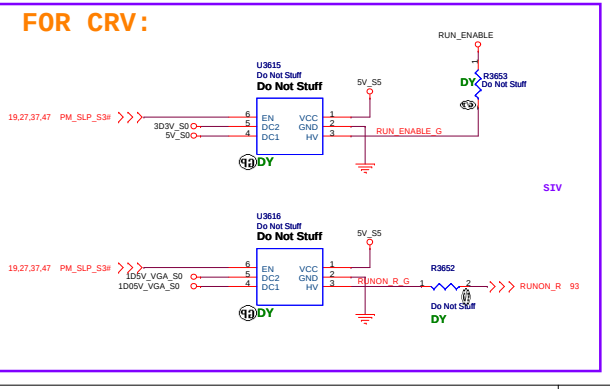


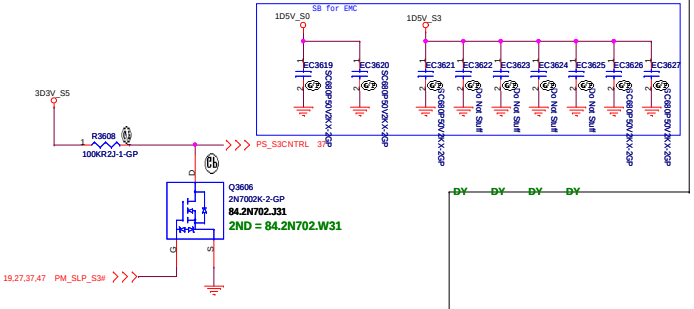


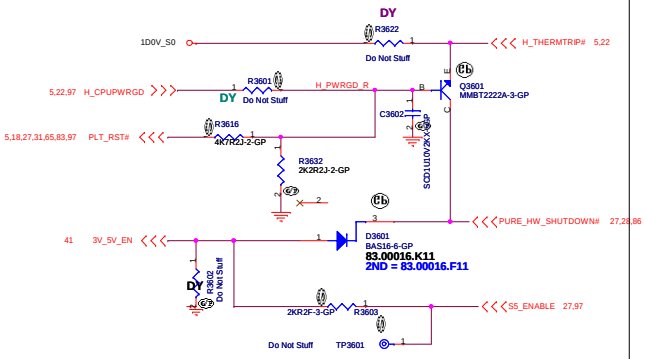
1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

FOR CRV:







BOM

緯創資通 **Wistron Corporation**
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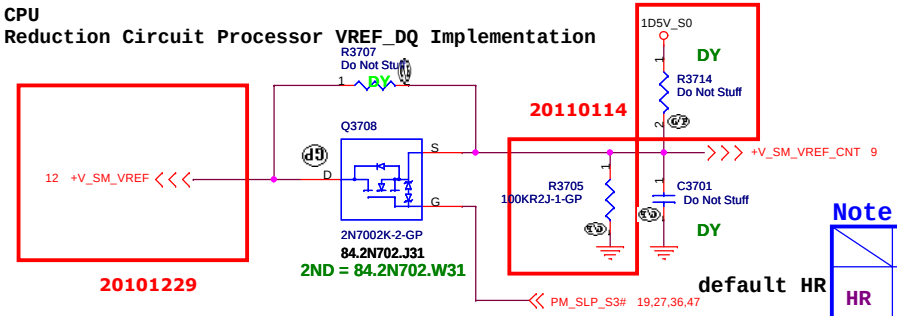
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PowerPlane Enable&Sequence**

Size	Document Number	Rev
	LG4858L	SB

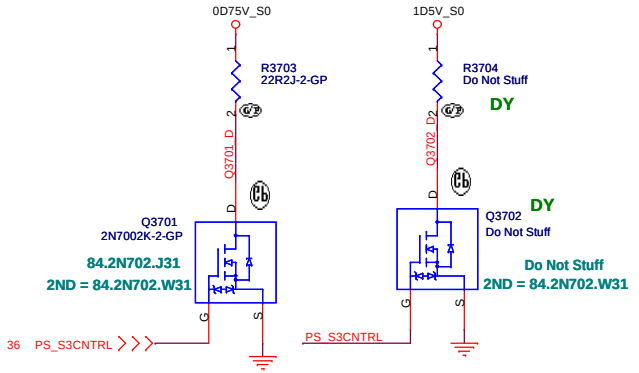
Date: Friday, March 16, 2012 Sheet 36 of 103

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



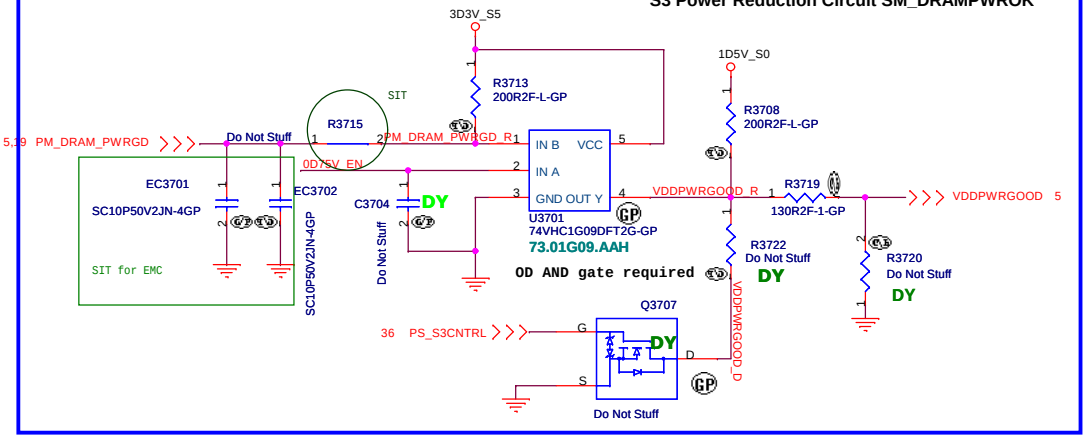
Note	R3705
HR	100K ohm 63.10434.1DL
CRV	1K ohm 64.10015.6DL

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



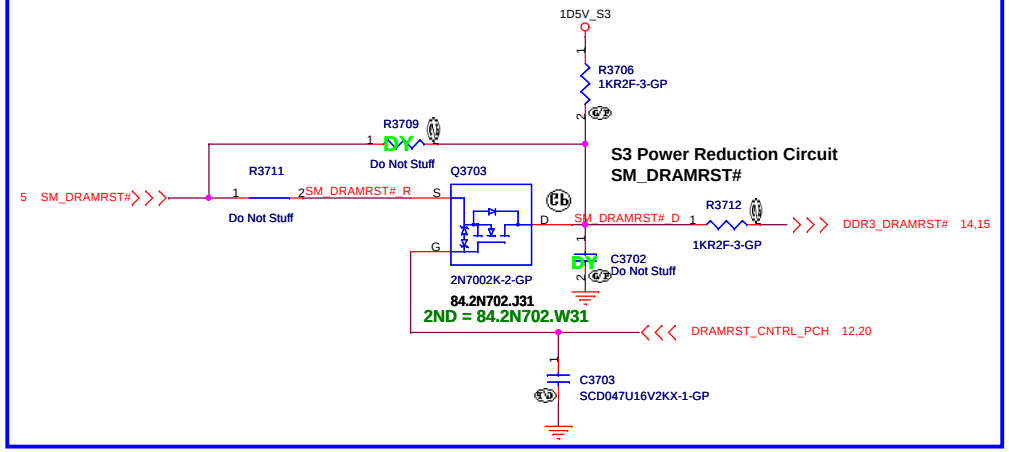
SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

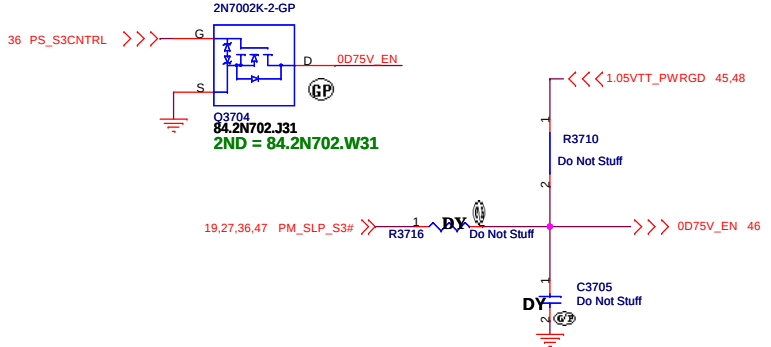


Do Not Stuff
2nd = 84.2N702.W31

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



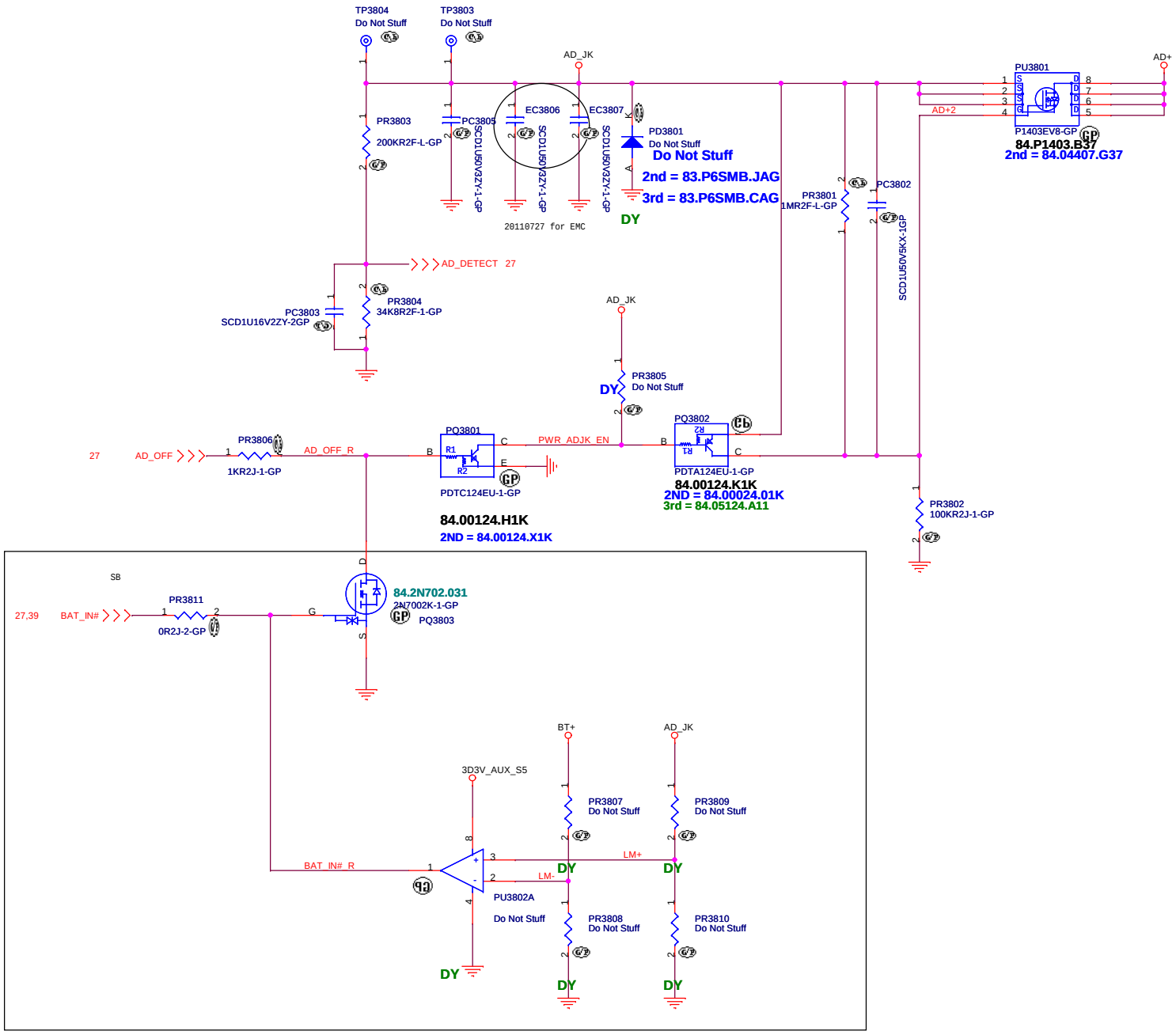
5 S3 Power Reduction



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADAPTER OCP / S3 reduction		
Size	Document Number: LG4858L	Rev: SB
Date: Friday, March 16, 2012	Sheet 37 of 103	

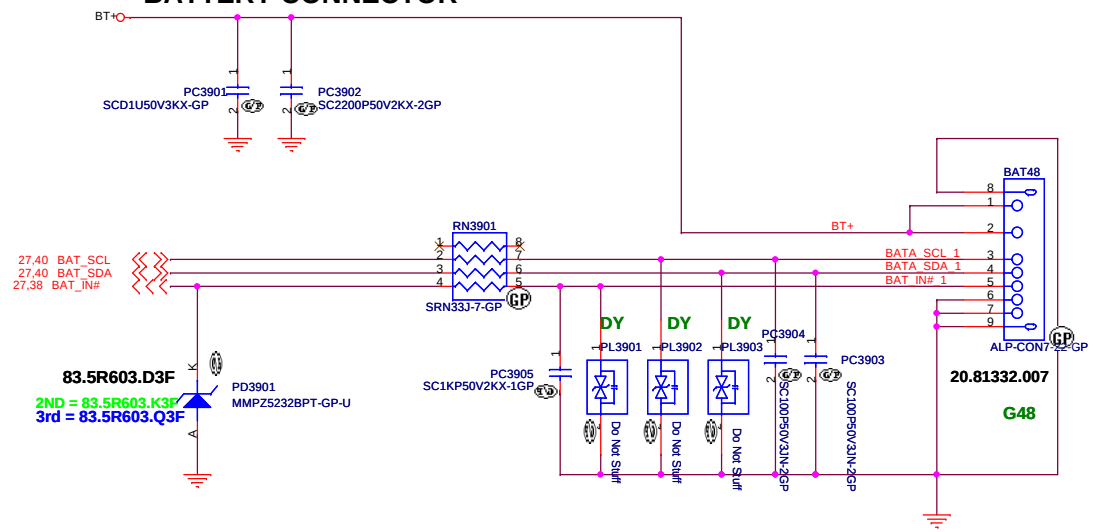
Adaptor in to generate DCBATOUT

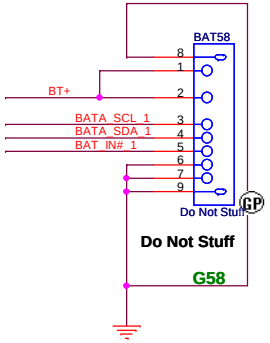


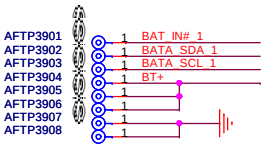
BOM

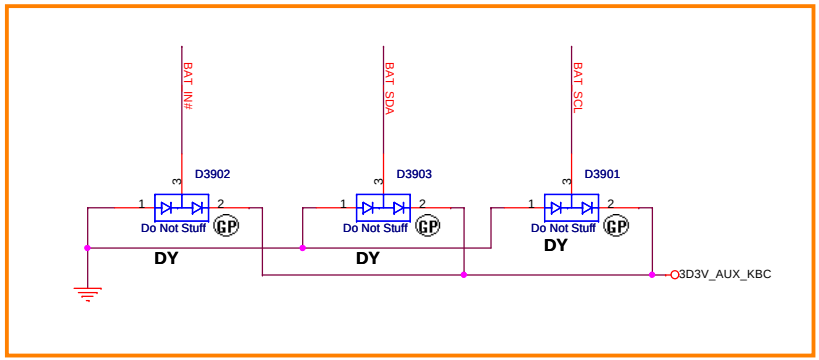
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN JACK***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 38 of 103	

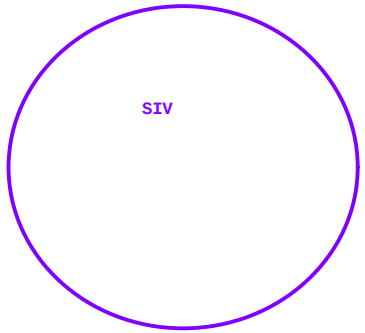
BATTERY CONNECTOR











BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BATT CONN***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 39 of 103	

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118k	100K

STOP_CHG#
connects to KBC

Charger Current=1.4~3.6A

PU4001 P1403EV8-GP
84.P1403.B37
2nd = 84.04407.G37
Id= -10A
Qg= -22nC
Rdson=14~22mohm

PU4002 P1403EV8-GP
84.P1403.B37
2nd = 84.04407.G37
Id= -10A
Qg= -22nC
Rdson=14~22mohm

PU4003 BQ24707ARGRR-GP

PU4004 P2003BEA-GP
84.02003.D37
2nd = 84.08067.A37

PU4005 P2003BEA-GP
84.02003.D37
2nd = 84.08067.A37

PQ4001 2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F

PQ4005 2N7002K-1-GP
84.2N702.031
2nd = 84.2N702.W31

PQ4009 2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F

PL4001 IND-5R6UH-48-GP-U1
68.5R610.10K
2nd = 68.5R610.30U

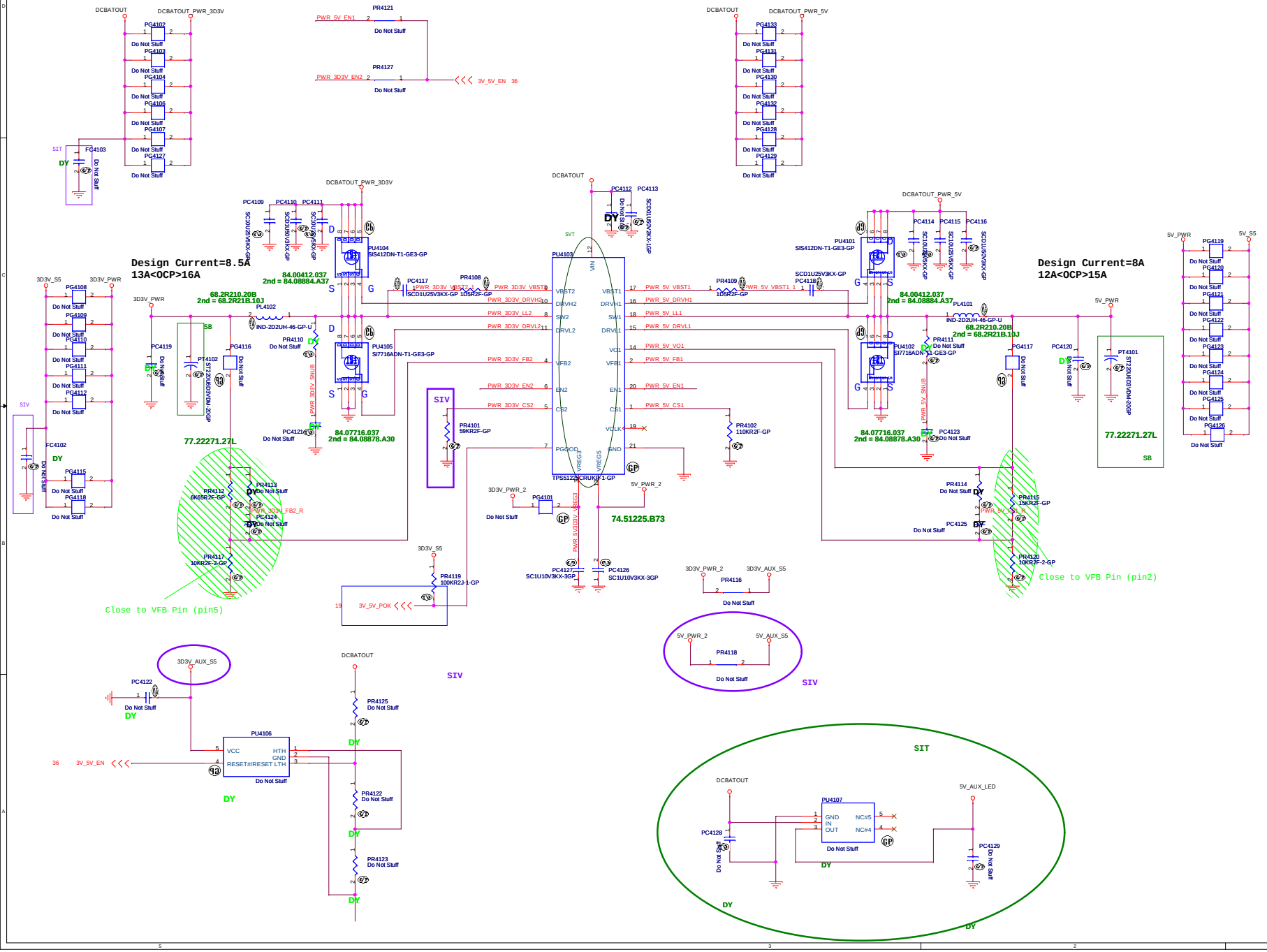
PD4003 CH520S-30PT-GP

PR4019 83.R0203.08F
2nd = 83.1R003.I8F

BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

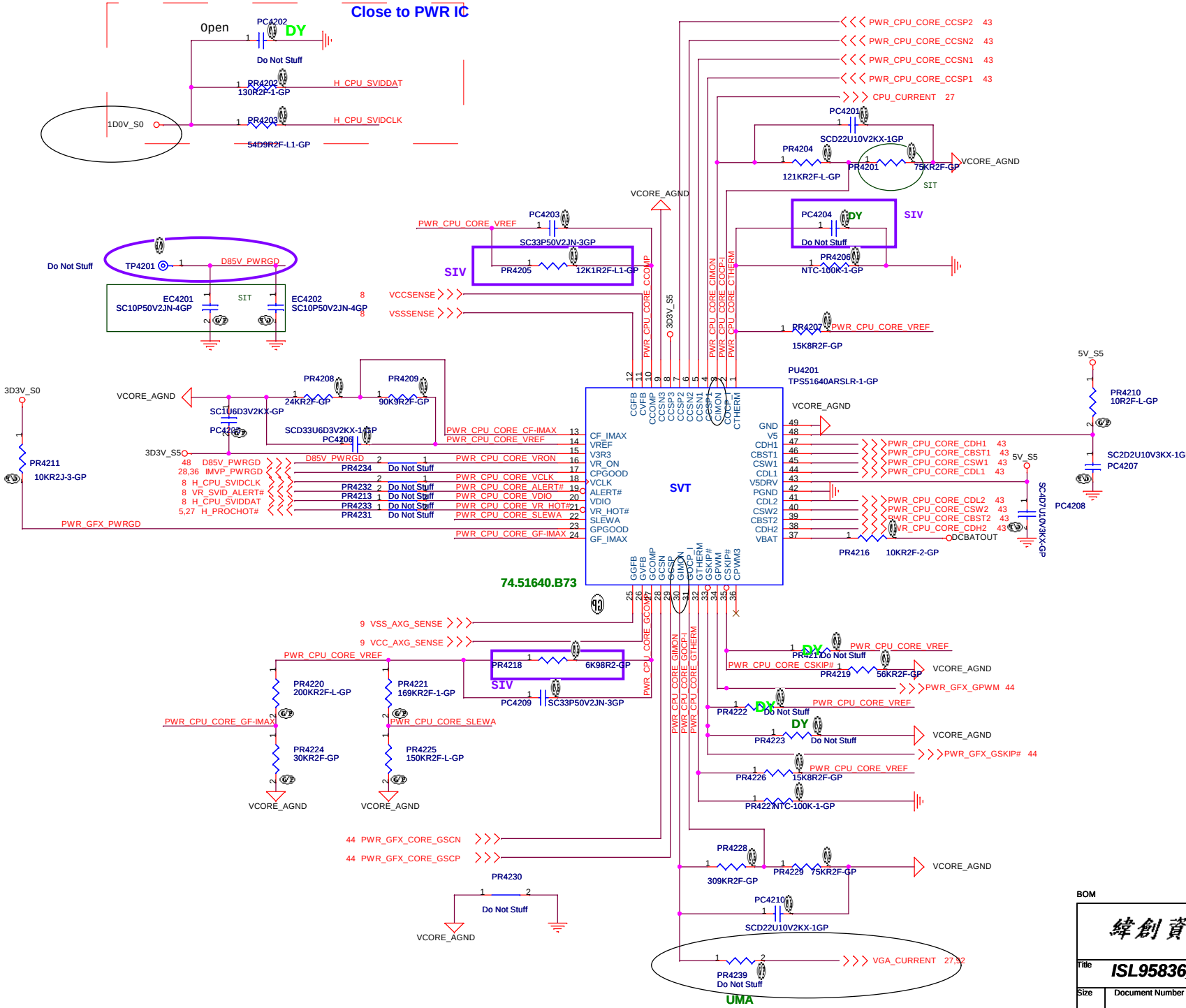
Title	BQ24745_Charger	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 40 of 103	

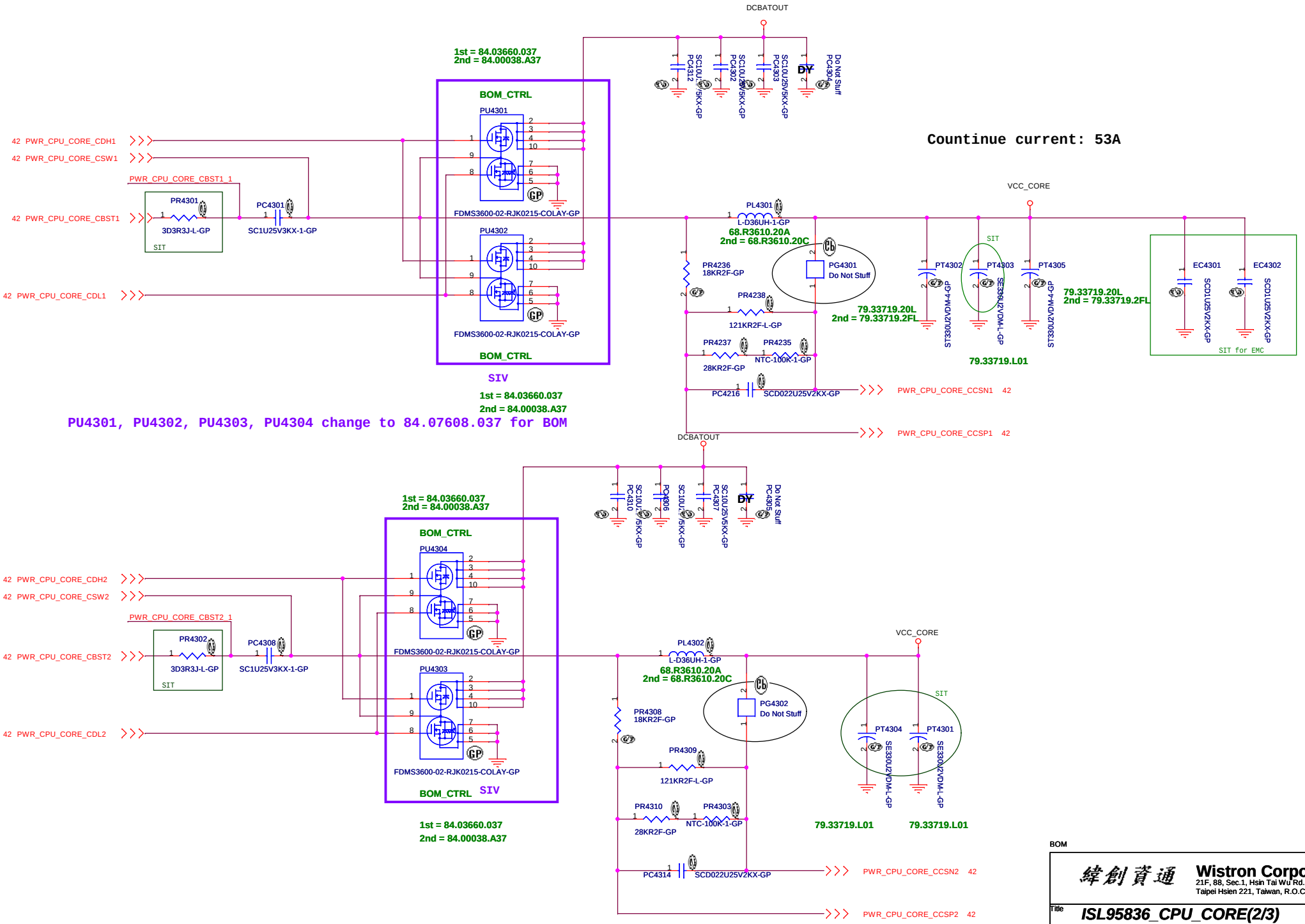
SSID = PWR.Plane.Regulator_5v3p3v



BOM

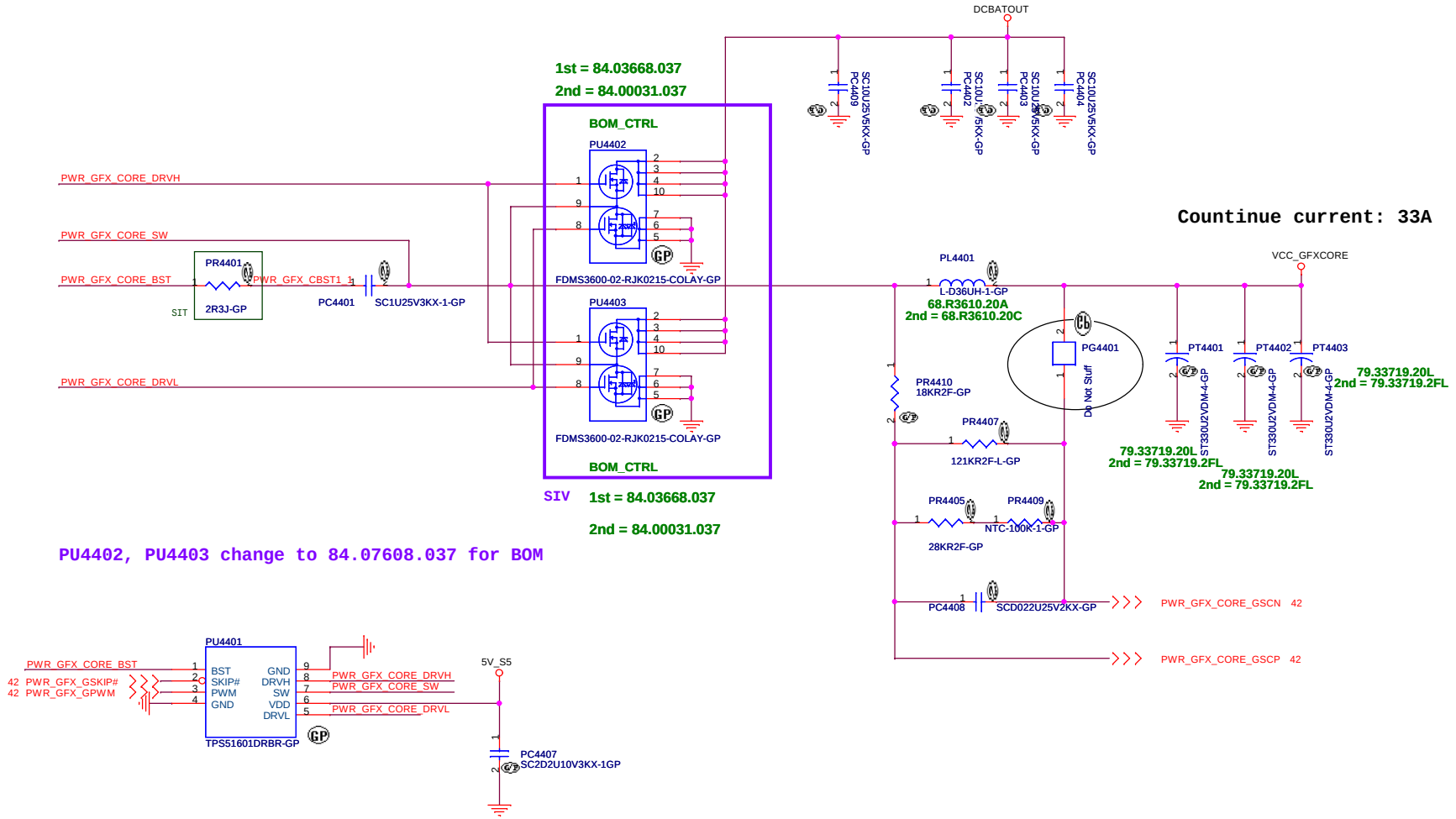
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	TPS51123_5V_3D3V	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 41 of 103	


Close to PWR IC
0pen
PC4202
DY
Do Not Stuff
PR4202
130R2F-1-GP
H_CPU_SVIDDAT
PR4203
54D9R2F-L1-GP
H_CPU_SVIDCLK
1D0V_S0
PWR_CPU_CORE_CCSP2 43
PWR_CPU_CORE_CCSN2 43
PWR_CPU_CORE_CCSN1 43
PWR_CPU_CORE_CCSP1 43
CPU_CURRENT 27
PC4201
SCD22U10V2KX-1GP
PR4204
121KR2F-L-GP
PR4201
75KR2F-GP
SIT
VCORE_AGND
VCORE_AGND
PC4204
DY
SIV
Do Not Stuff
PR4206
NTC-100K-1-GP
PWR_CPU_CORE_VREF
PC4203
SC33P50V2JN-3GP
PR4205
12K1R2F-L1-GP
SIV
Do Not Stuff
TP4201
D85V_PWRGD
EC4201
SC10P50V2JN-4GP
SIT
EC4202
SC10P50V2JN-4GP
VCCSENSE 8
VSSSENSE 8
PR4207
15K8R2F-GP
PWR_CPU_CORE_VREF
PU4201
TPS51640ARSLR-1-GP
3D3V_S0
PR4211
10KR2J-3-GP
PR4208
24KR2F-GP
PR4209
90K9R2F-GP
SC1U6D3V2KX-GP
PC4205
SCD33U6D3V2KX-1GP
PC4206
3D3V_S5
PWR_GFX_PWRGD
PWR_CPU_CORE_CF-IMAX
PWR_CPU_CORE_VREF
PWR_CPU_CORE_VRON
PWR_CPU_CORE_VCLK
PWR_CPU_CORE_ALERT#
PWR_CPU_CORE_VDIO
PWR_CPU_CORE_VR_HOT#
PWR_CPU_CORE_SLEWA
PWR_CPU_CORE_GF-IMAX
48 D85V_PWRGD
28,36 IMVP_PWRGD
8 H_CPU_SVIDCLK
8 VR_SVID_ALERT#
8 H_CPU_SVIDDAT
5,27 H_PROCHOT#
PR4234 Do Not Stuff
PR4232 Do Not Stuff
PR4213 Do Not Stuff
PR4233 Do Not Stuff
PR4231 Do Not Stuff
CF_IMAX
VREF
V3R3
VR_ON
CPGOOD
VCLK
ALERT#
VDIO
VR_HOT#
SLEWA
GPGOOD
GF_IMAX
SVT
GND
V5
CDH1
CBST1
CSW1
CDL1
V5DRV
PGND
CDL2
CSW2
CBST2
CDH2
VBAT
PWR_CPU_CORE_CDH1 43
PWR_CPU_CORE_CBST1 43
PWR_CPU_CORE_CSW1 43
PWR_CPU_CORE_CDL1 43
PWR_CPU_CORE_CDL2 43
PWR_CPU_CORE_CSW2 43
PWR_CPU_CORE_CBST2 43
PWR_CPU_CORE_CDH2 43
DCBATOUT
PR4216
10KR2F-2-GP
5V_S5
PR4210
10R2F-L-GP
SC2D2U10V3KX-1GP
PC4207
PC4208
SC4D7U10V3KX-GP
74.51640.B73
9 VSS_AXG_SENSE
9 VCC_AXG_SENSE
PR4218
6K98R2-GP
SIV
PC4209
SC33P50V2JN-3GP
PR4220
200KR2F-L-GP
PR4221
169KR2F-1-GP
PR4224
30KR2F-GP
PR4225
150KR2F-L-GP
PWR_CPU_CORE_GF-IMAX
PWR_CPU_CORE_SLEWA
VCORE_AGND
VCORE_AGND
PR4230
Do Not Stuff
VCORE_AGND
44 PWR_GFX_CORE_GSCN
44 PWR_GFX_CORE_GSCP
PR4211
DY
Do Not Stuff
PWR_CPU_CORE_CSKIP#
PR4219
56KR2F-GP
PWR_GFX_GPWM 44
PR4222
DY
Do Not Stuff
PR4223
DY
Do Not Stuff
PWR_GFX_SKIP# 44
PR4226
15K8R2F-GP
PR4227
NTC-100K-1-GP
PR4228
309KR2F-GP
PR4229
75KR2F-GP
PC4210
SCD22U10V2KX-1GP
PR4239
Do Not Stuff
VGA_CURRENT 27,32
UMA
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL95836_CPU_CORE(1/3)
Size
Document Number
LG4858L
Rev
SB
Date: Friday, March 16, 2012
Sheet 42 of 103



BOM

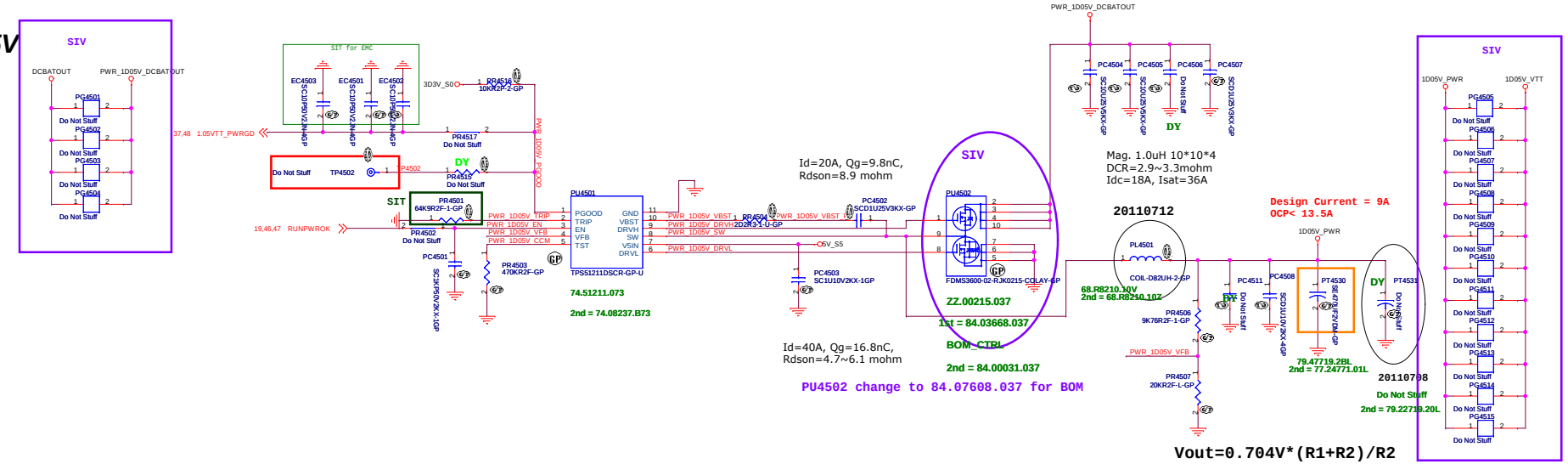
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ISL95836_CPU_CORE(2/3)***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 43 of 103	



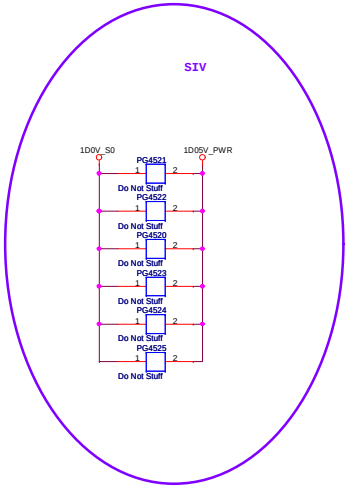
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*ISL95836_CPU_CORE(3/3)*	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 44 of 103	

TPS51211 for 1D05V



APL5916 for 1D0V

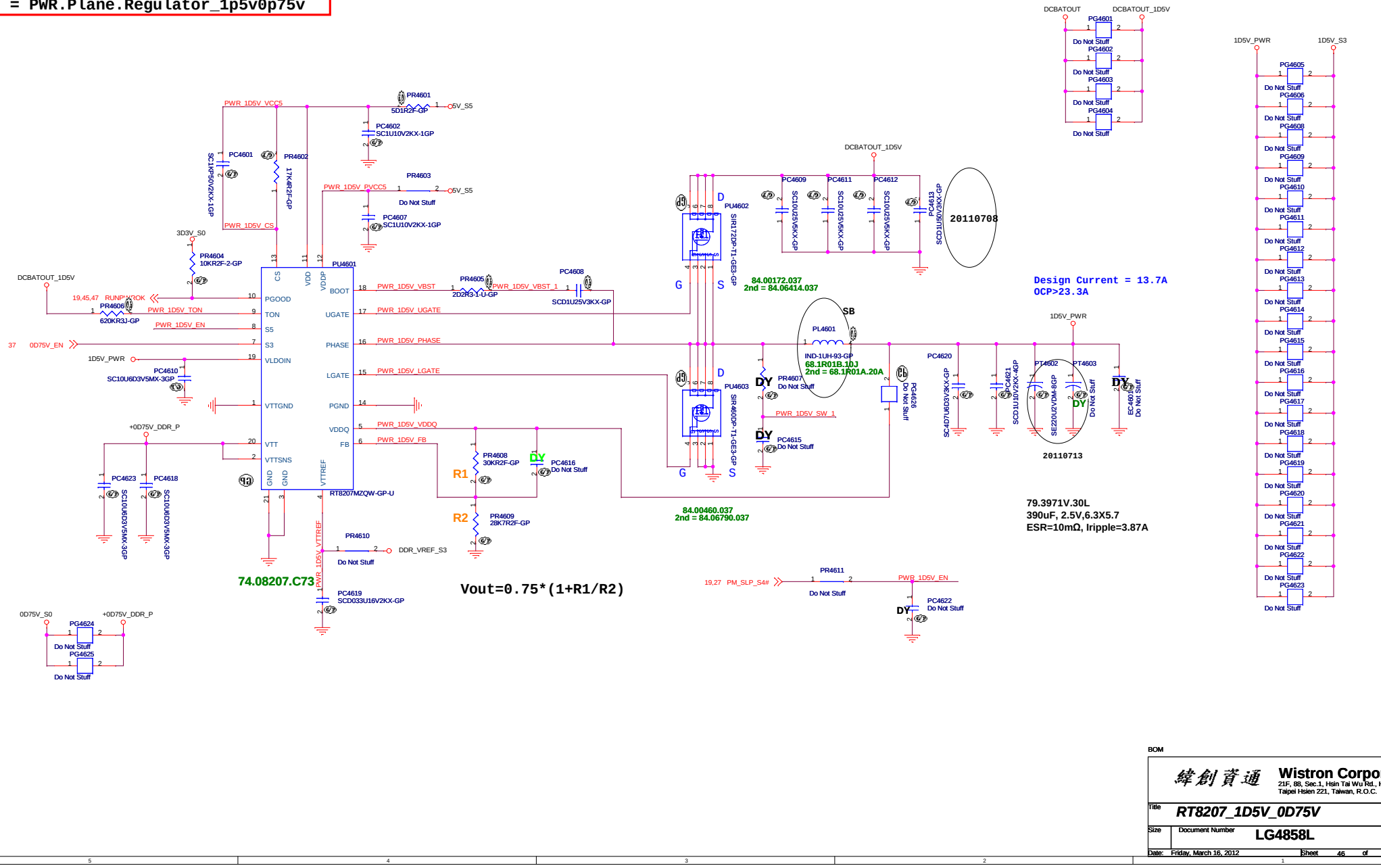


BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51211_1D05V&TPS51219_1D0V	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 45 of 103	

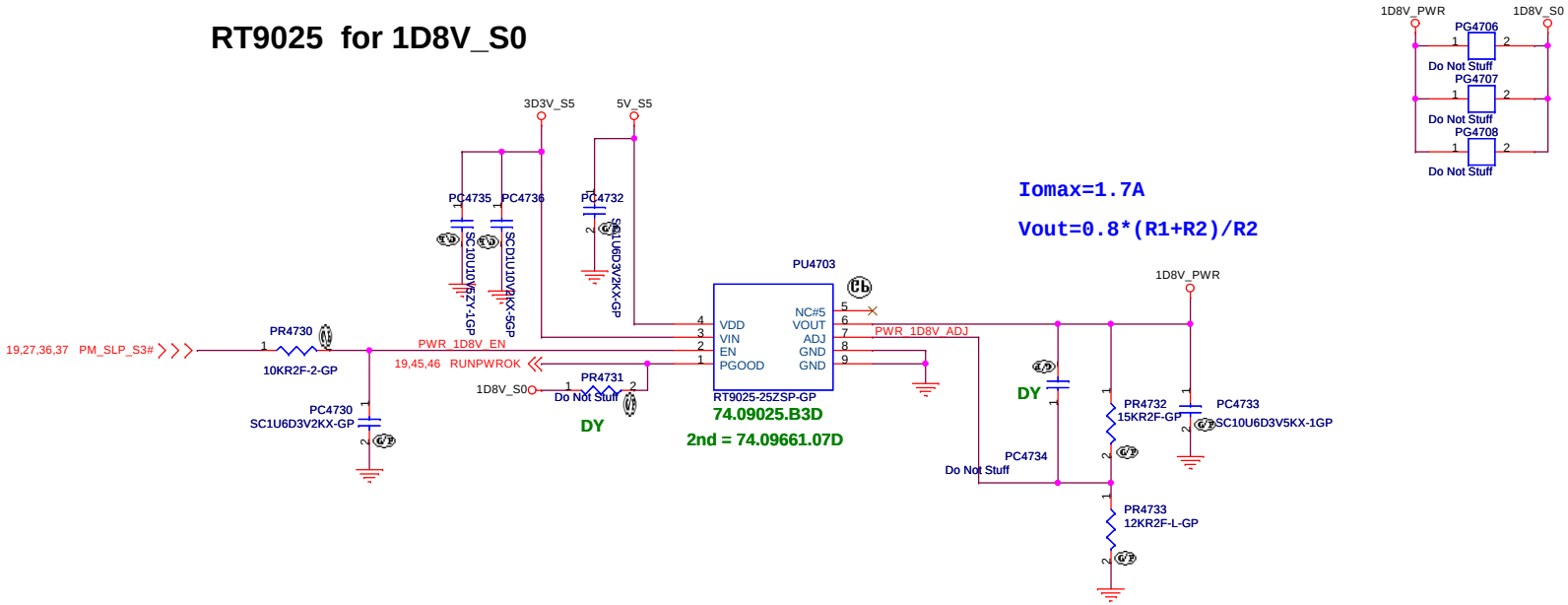
SSID = PWR.Plane.Regulator_1p5v0p75v



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT8207_1D5V_0D75V***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 46 of 103	

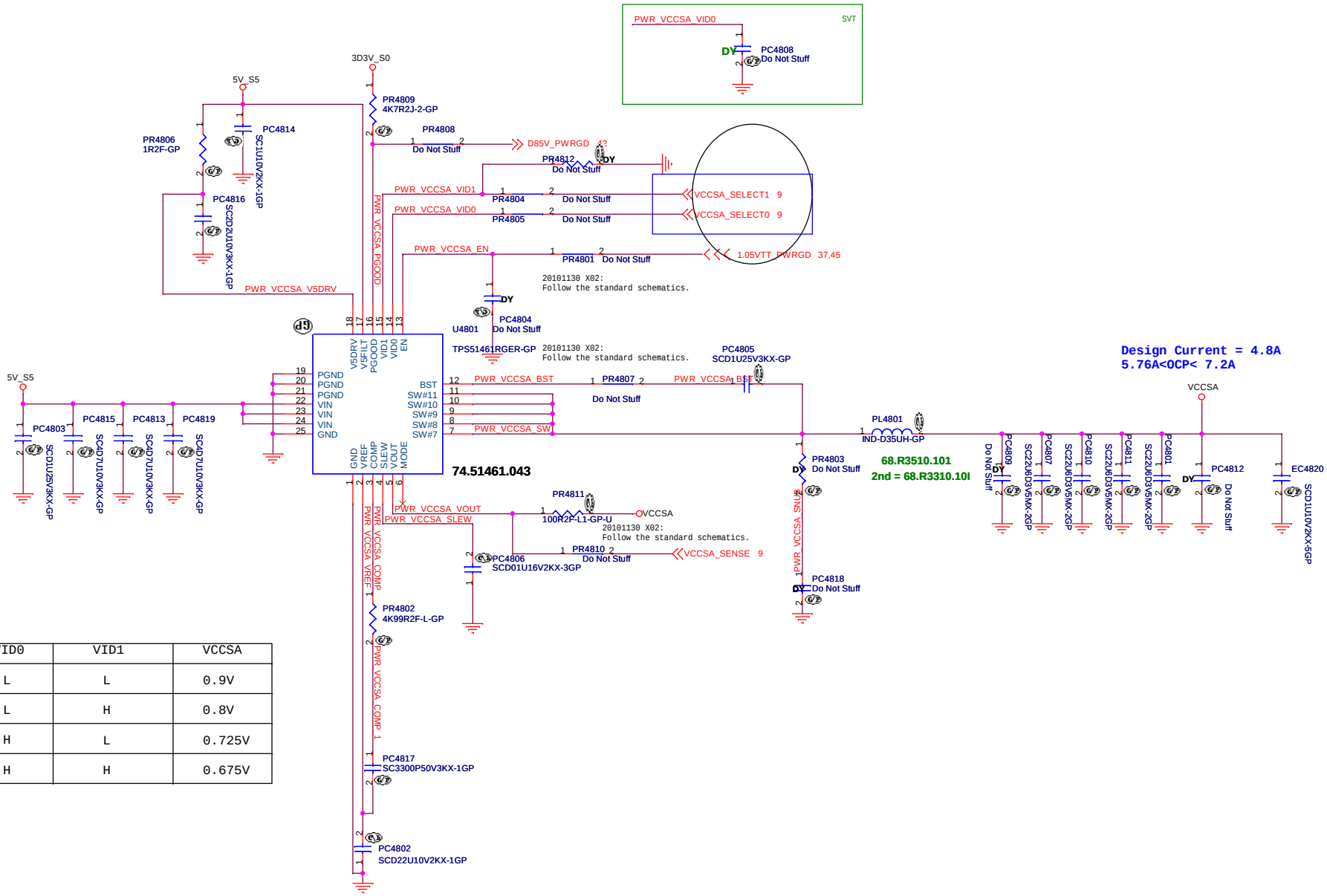
RT9025 for 1D8V_S0



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RT9205_1D8V*		
Size	Document Number: **LG4858L**	Rev: **SB**
Date: Friday, March 16, 2012	Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

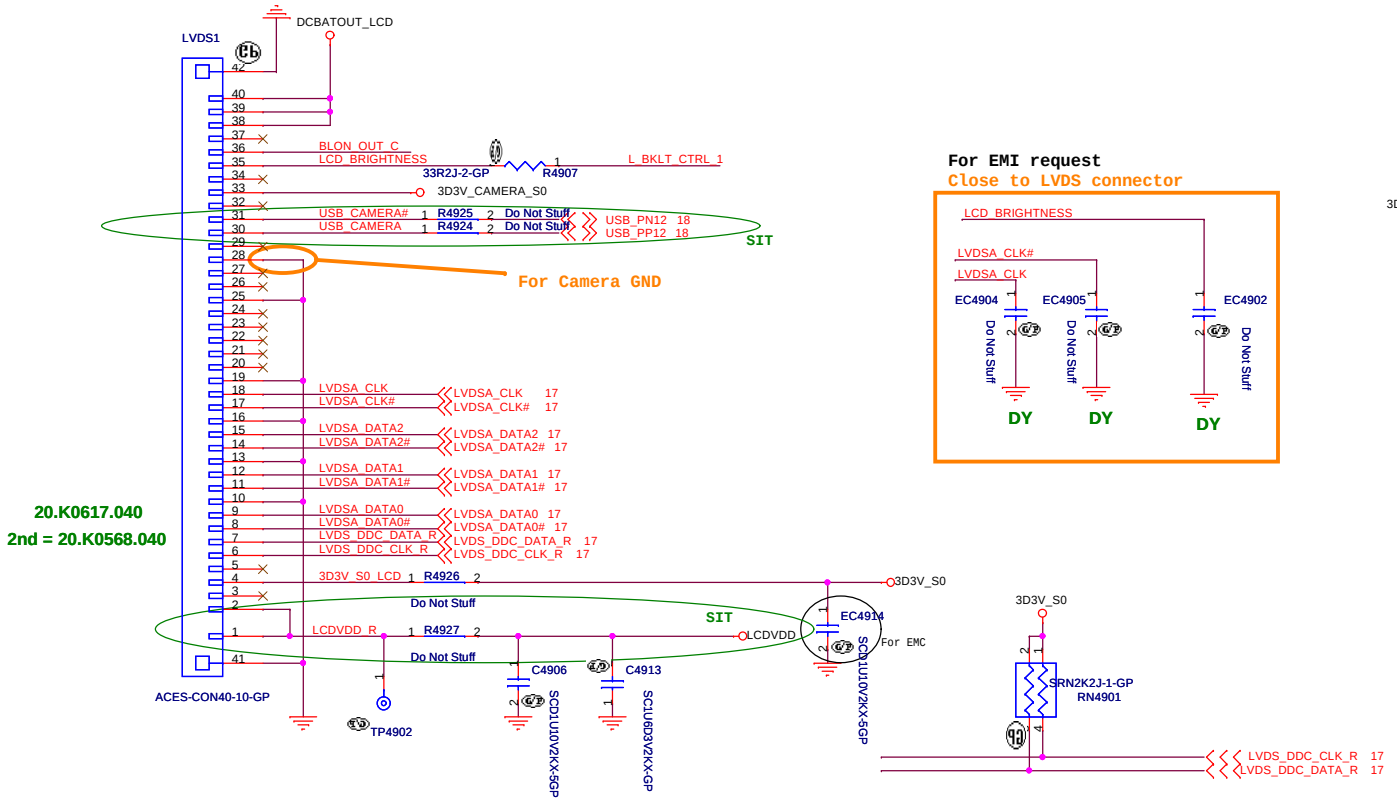
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VCCSA_TPS51461*	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 48 of 103	

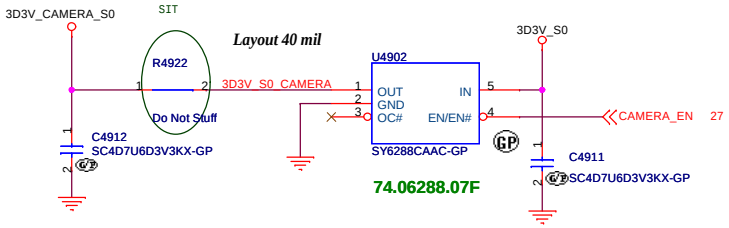
SSID = VIDEO

LVDS connector



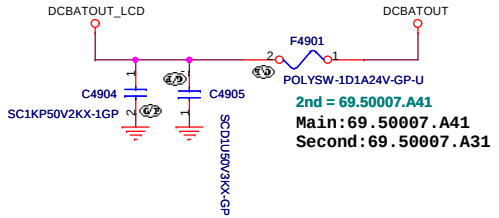
For EMI request
Close to LVDS connector

CAMERA POWER

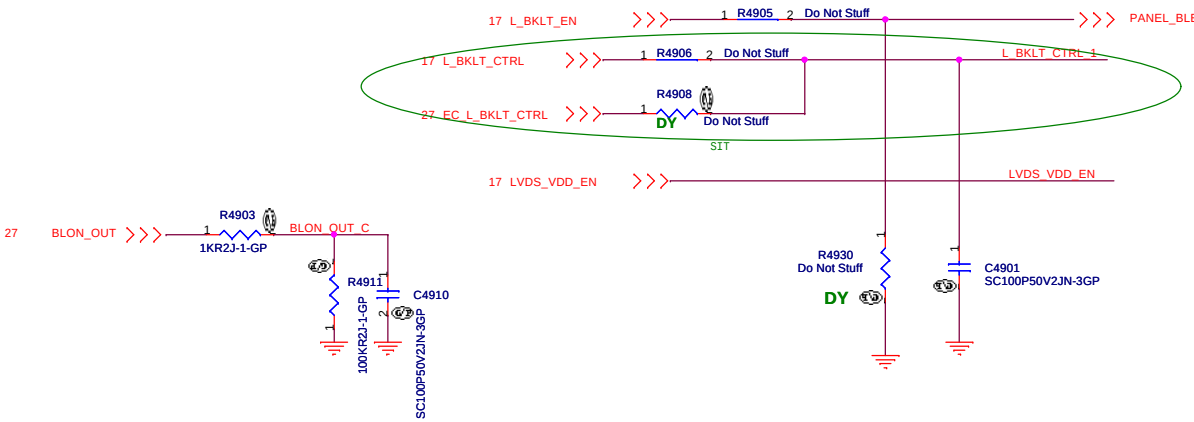


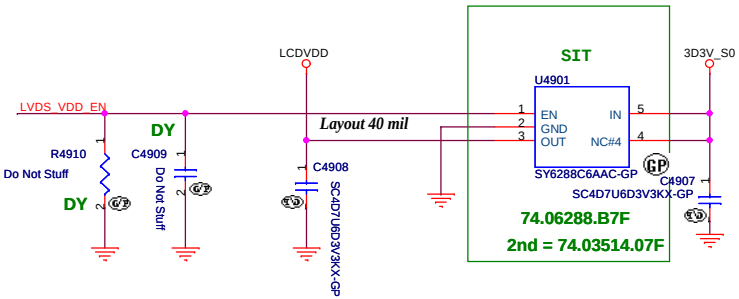
U4902 Change to 74.07534 from 74.05240.A7F for obsoleted part

LCD POWER



Panel BL brightness/Power En/BL En



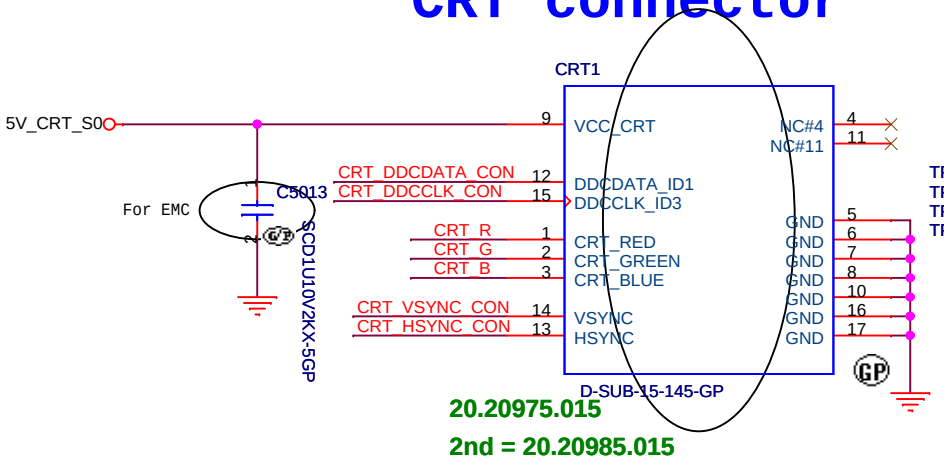


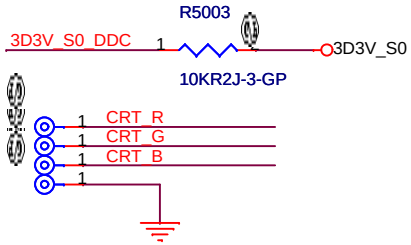
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*LCD/Inverter Connector*	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 49 of 103	

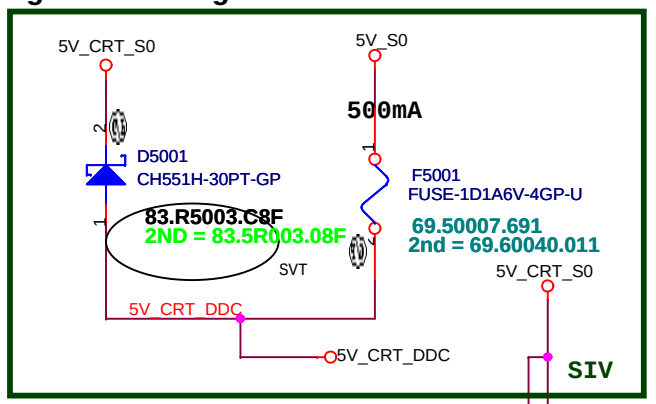
CRT connector



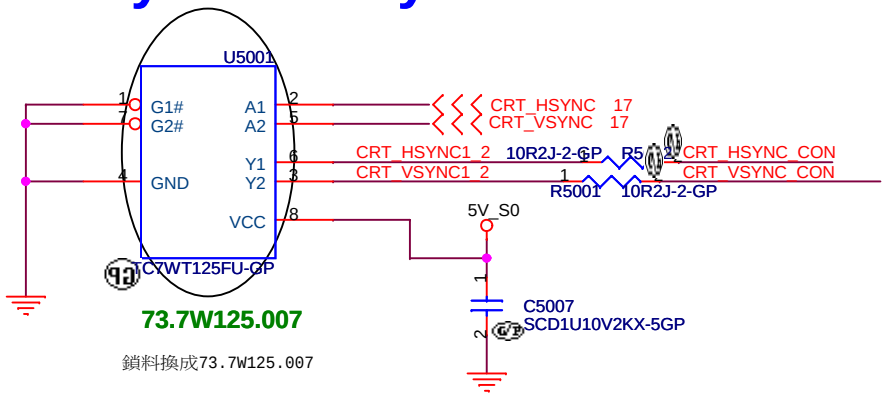


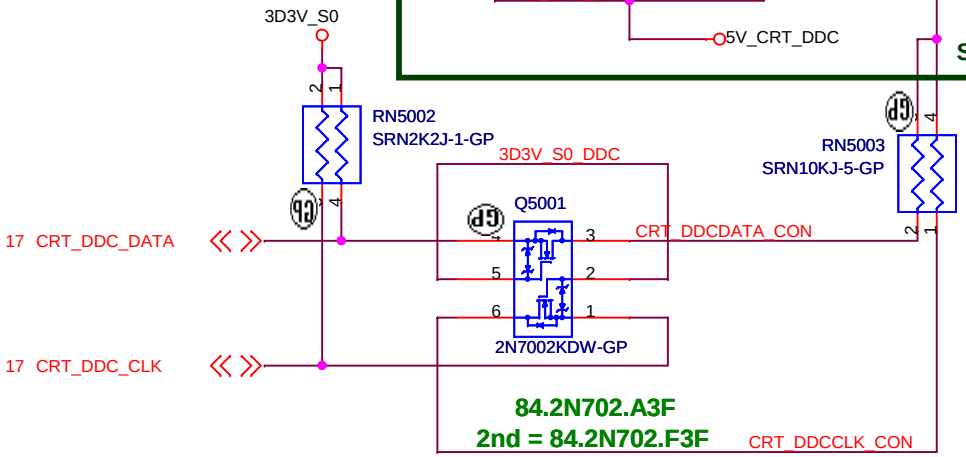
CRT DDCDATA & DDCCLK level shift

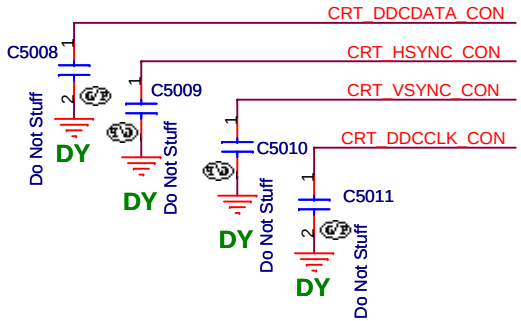
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

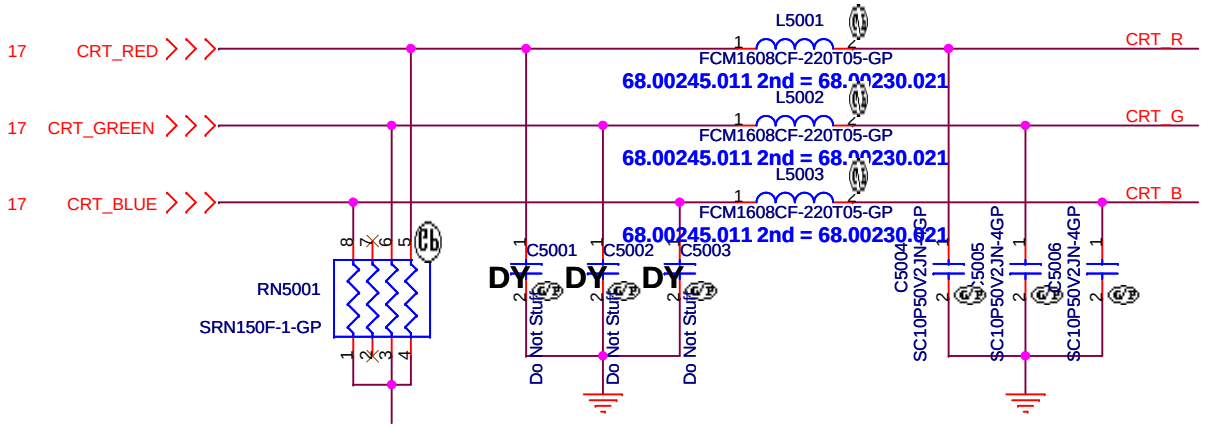






CRT RGB

R,G,B place 22pF and ESD diode for intel check list



BOM

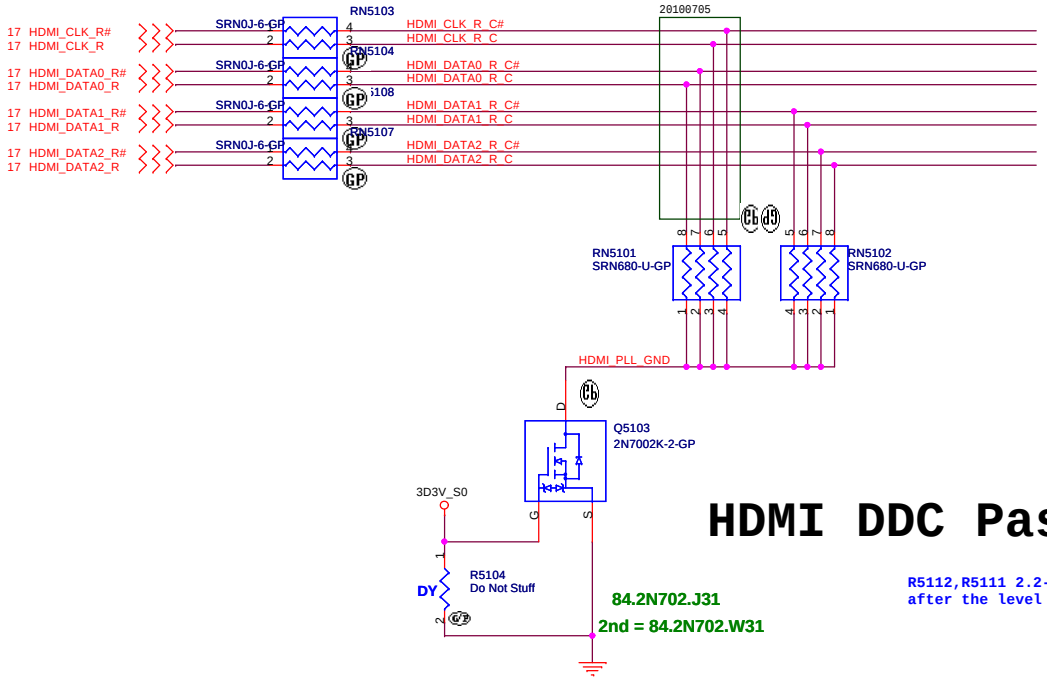
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Board Connector***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 50 of 103	

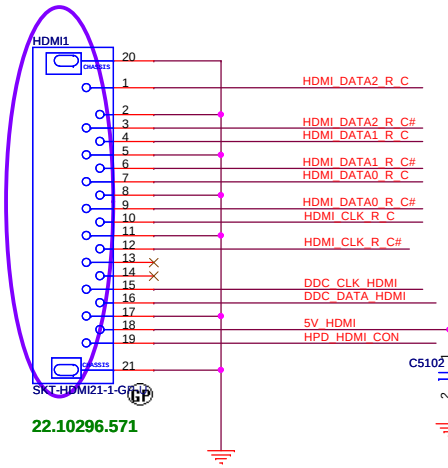
SSID = VIDEO

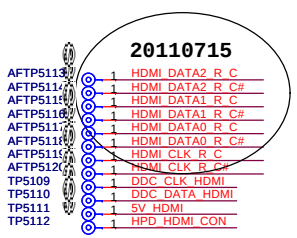
HDMI CONNECTOR

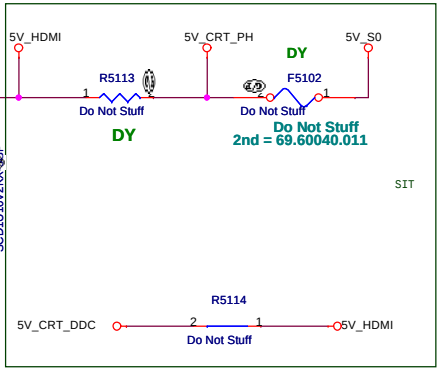
HDMI Passive Level Shifter

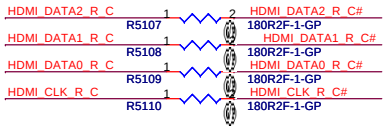
Close to HDMI Connector





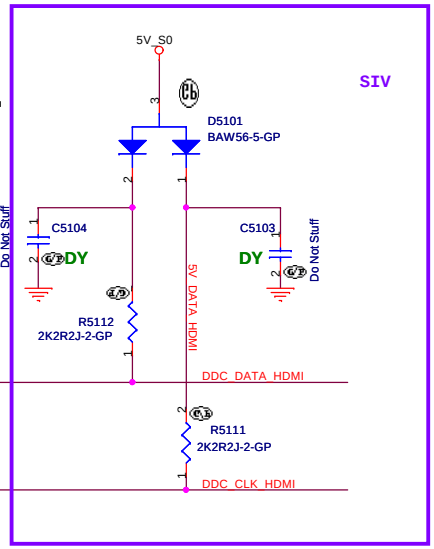


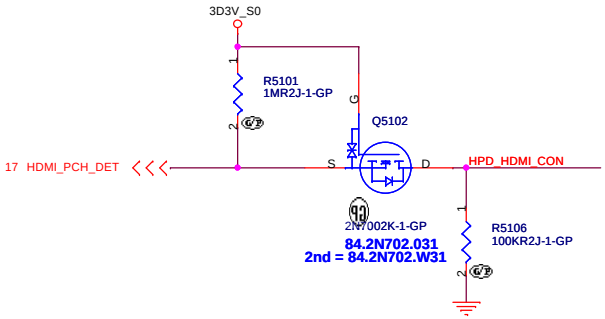


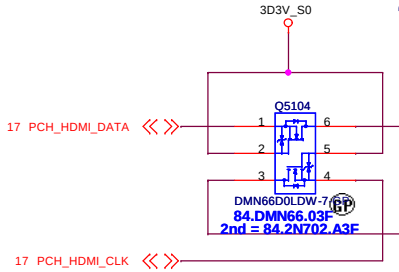


HDMI DDC Passive Level Shifter

R5112,R5111 2.2-kΩ ±5% pull-up to 5 V
after the level shifter for intel check list





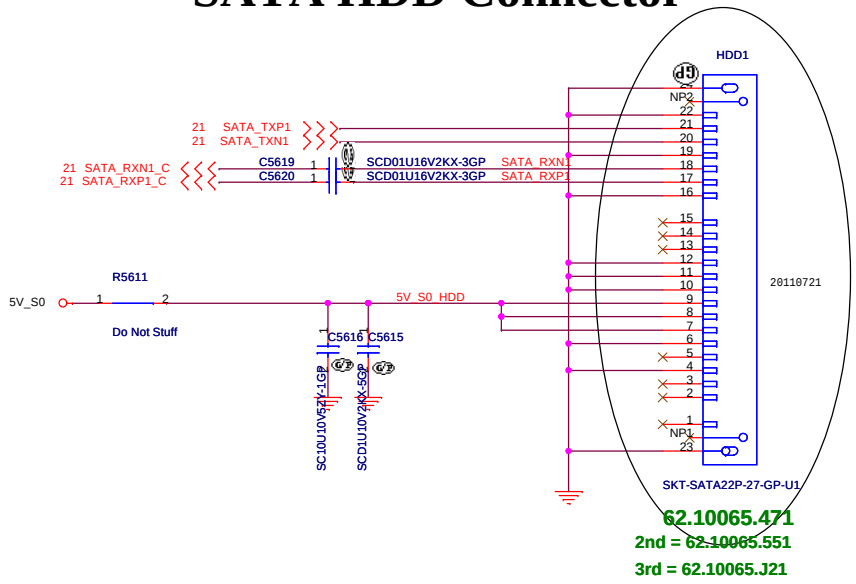


BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Conn	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 51 of 103	

SSID = SATA

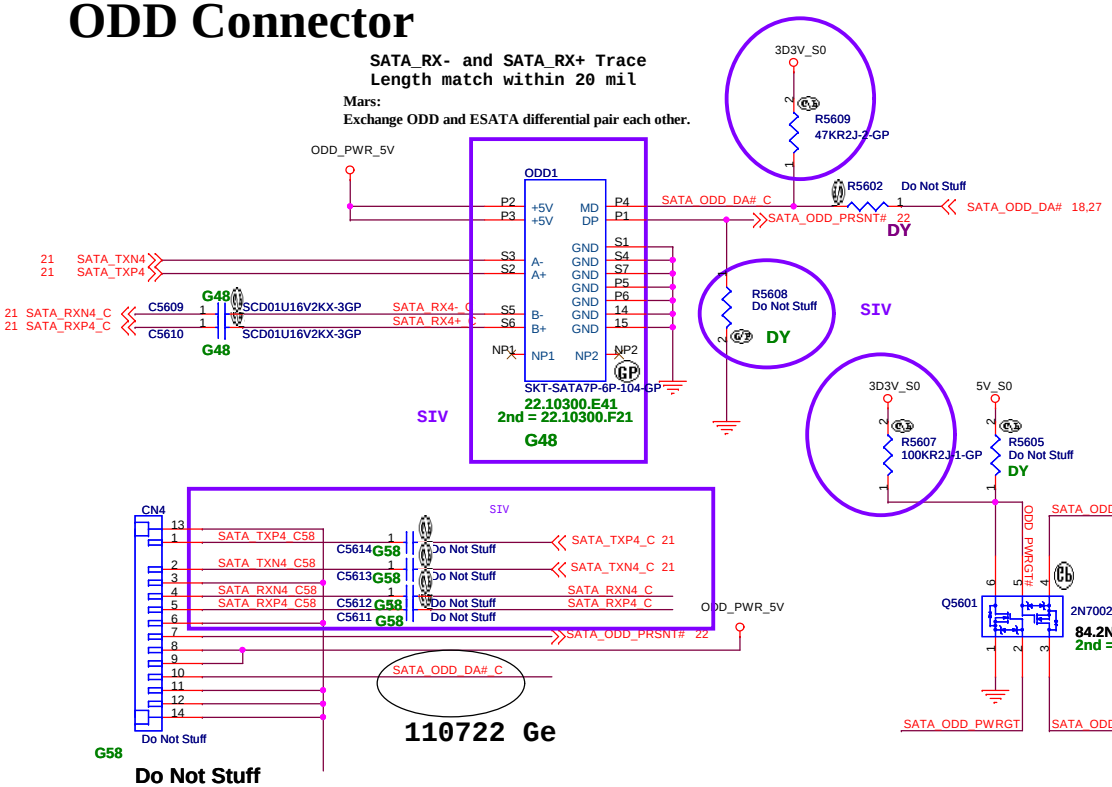
SATA HDD Connector



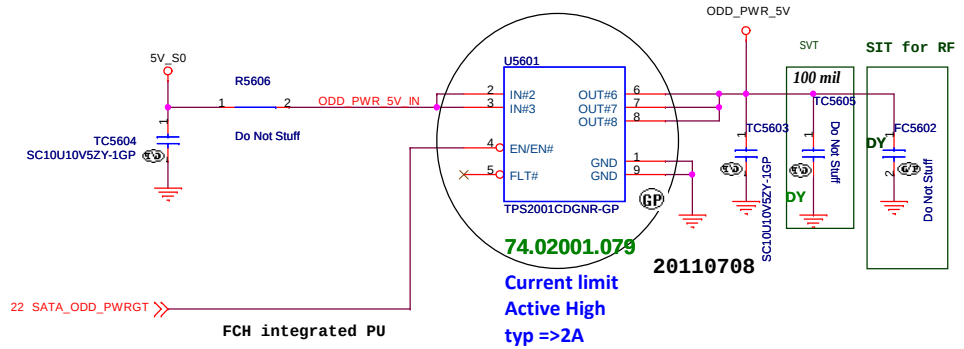
ODD Connector

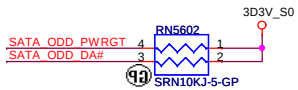
SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD



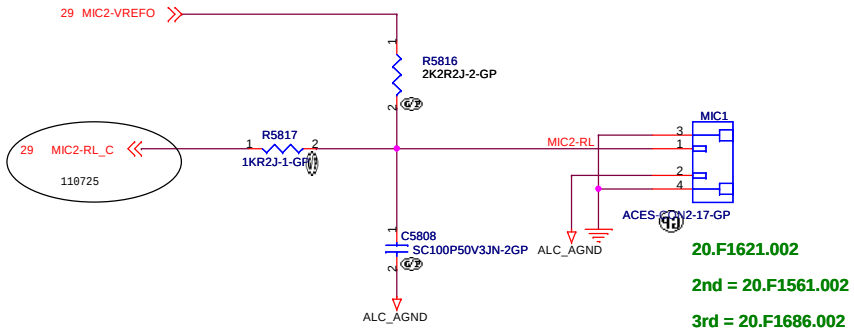


SUPPORT ZERO SATA ODD

BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size	Document Number: LG4858L	Rev: SB
Date: Friday, March 16, 2012	Sheet 56 of 103	

Analog Internal Mic



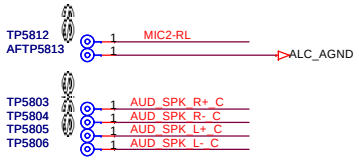
20.F1621.002

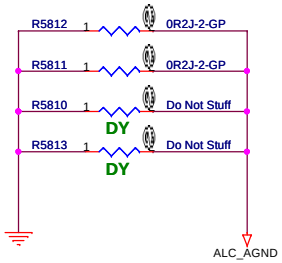
2nd = 20.F1561.002

3rd = 20.F1686.002

4nd = 20.F0693.002

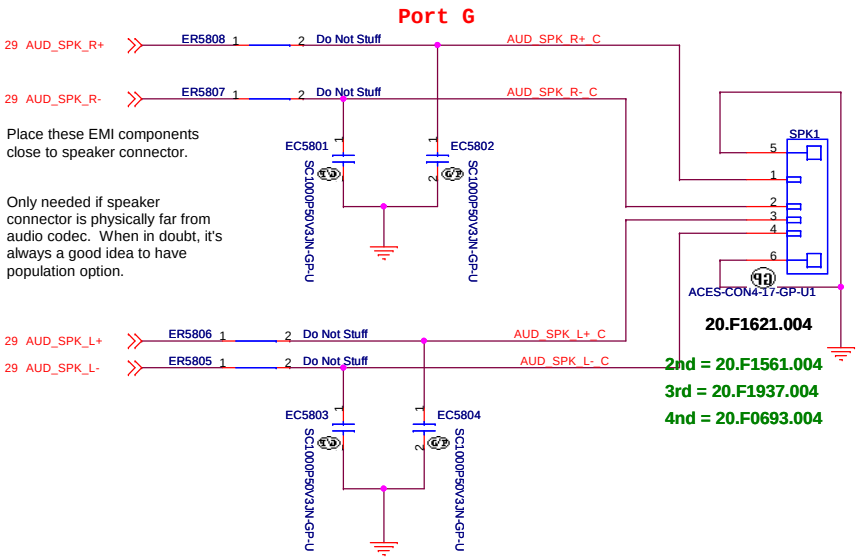
For EMI request:
Change C5801,C5802 to varister 69.80024.001





SIV
Remove bestbuy

INTERNAL STEREO SPEAKERS



20.F1621.004

2nd = 20.F1561.004

3rd = 20.F1937.004

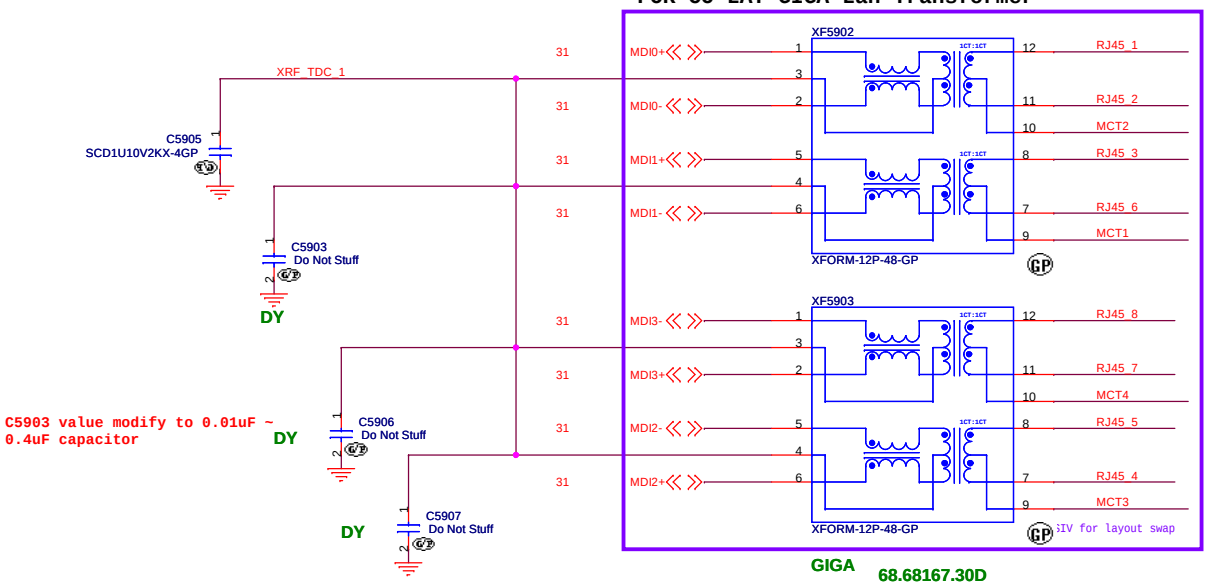
4nd = 20.F0693.004

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MIC/SPEAKER/AUDIO JACK	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 58 of 103	

10/100M Lan Transformer



68.68167.30D

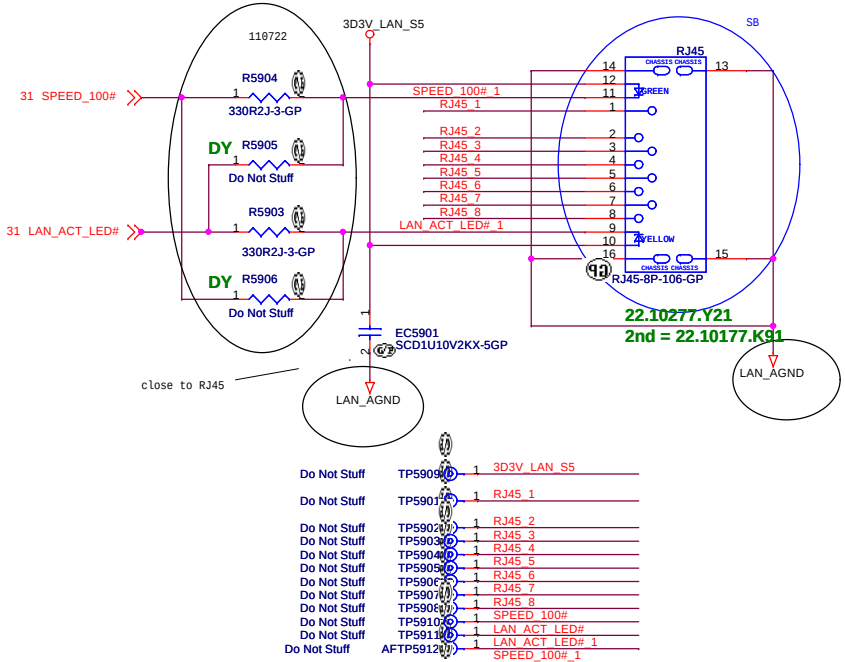
2nd = 68.0NS14.301

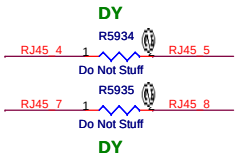
3rd = 68.HD081.30B

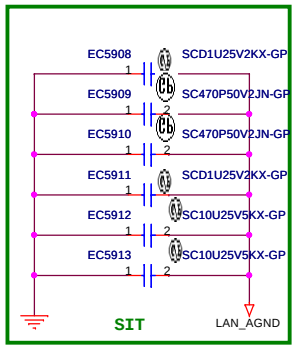
1.route as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For AR8162(10/100M): C5906, C5907,R5938, R5939 can be DY.
For AR8161(GIGA): Dummy R5934, R5935, R5940,R5941

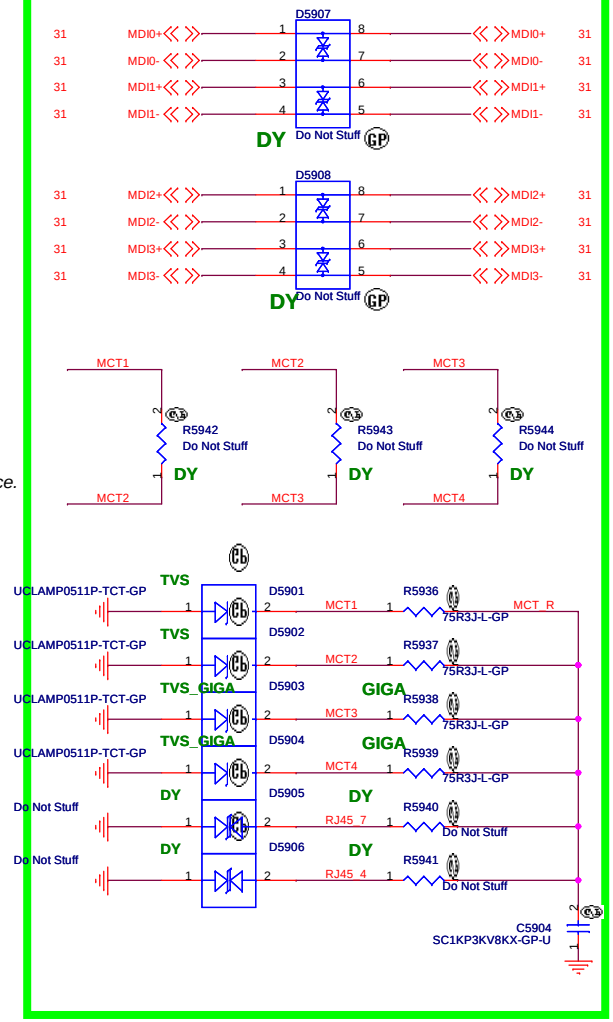
LAN Connector







10/100 LAN surge circuit

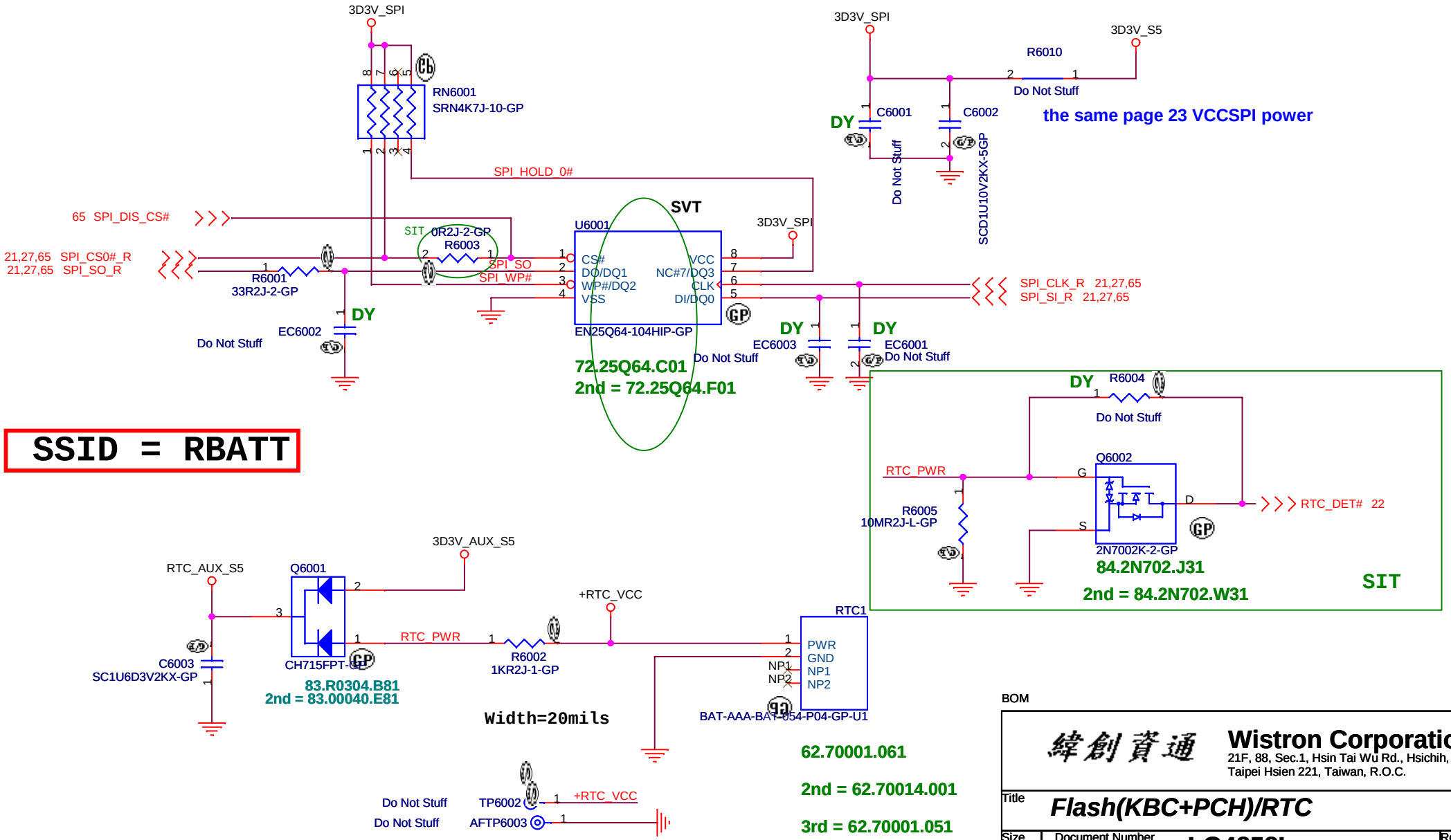


BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RJ45		
Size	Document Number: LG4858L	Rev: SB
Date: Friday, March 16, 2012	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

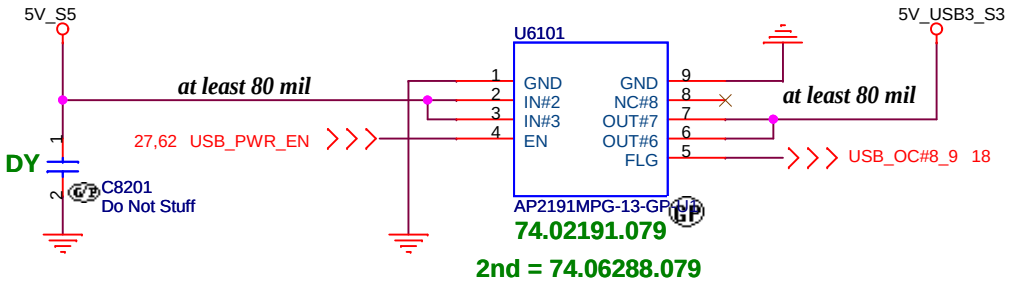


BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Flash(KBC+PCH)/RTC***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 60 of 103	

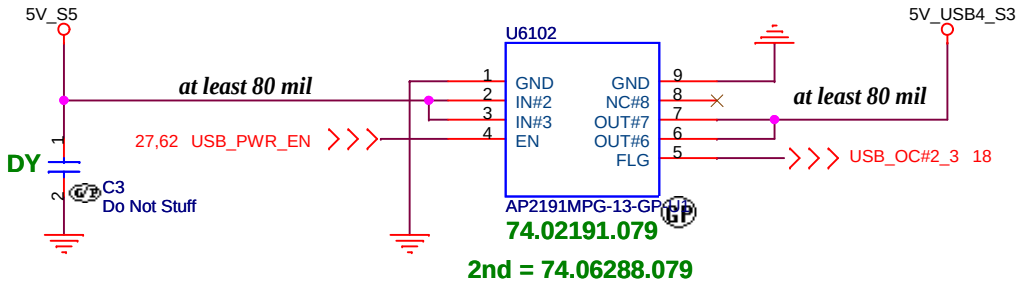
SSID = USB

USB Ext. port3 power SW



U6101 place near to USBCN3

USB Ext. port4 power SW



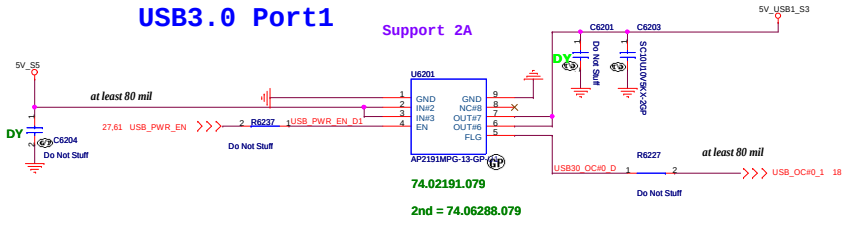
U6102 place near to CDRCN2

BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: *USB2.0 Port Power SW*			
Size	Document Number: **LG4858L**		Rev: **SB**
Date: Friday, March 16, 2012		Sheet 61 of 103	

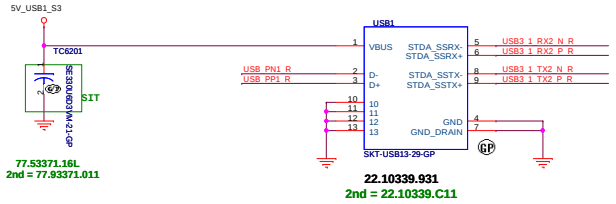
USB3.0 Port1

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

2nd = 77.93371.011

22.10339.931

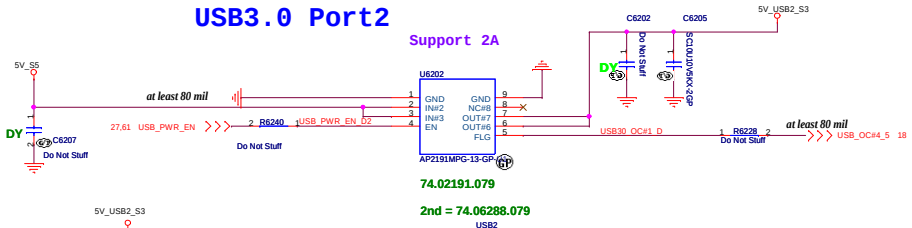
2nd = 22.10339.C11

TC6201 place near
the USB1 connector

Co-Layout USB2.0 22.10321.S01

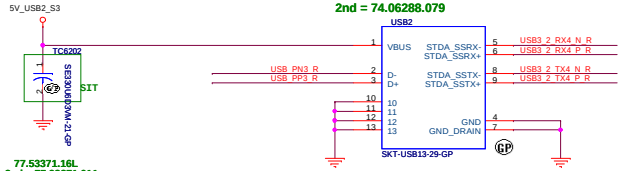
USB3.0 Port2

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

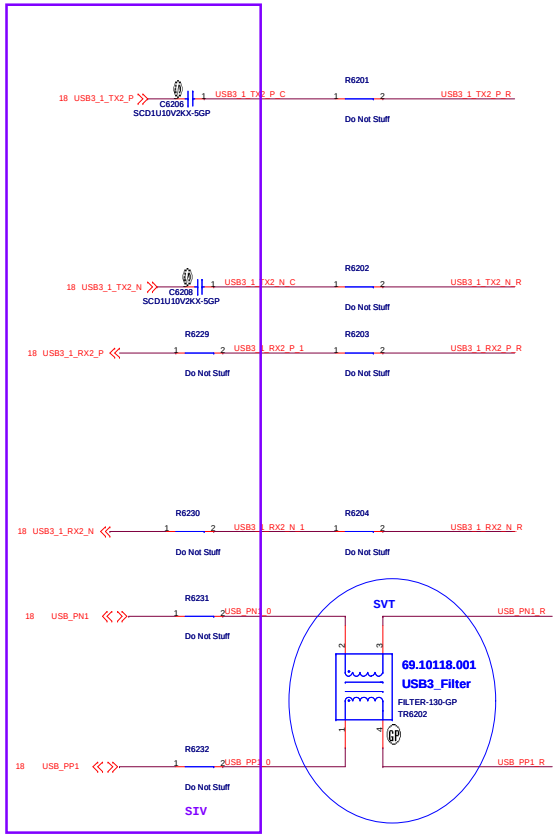
2nd = 77.93371.011

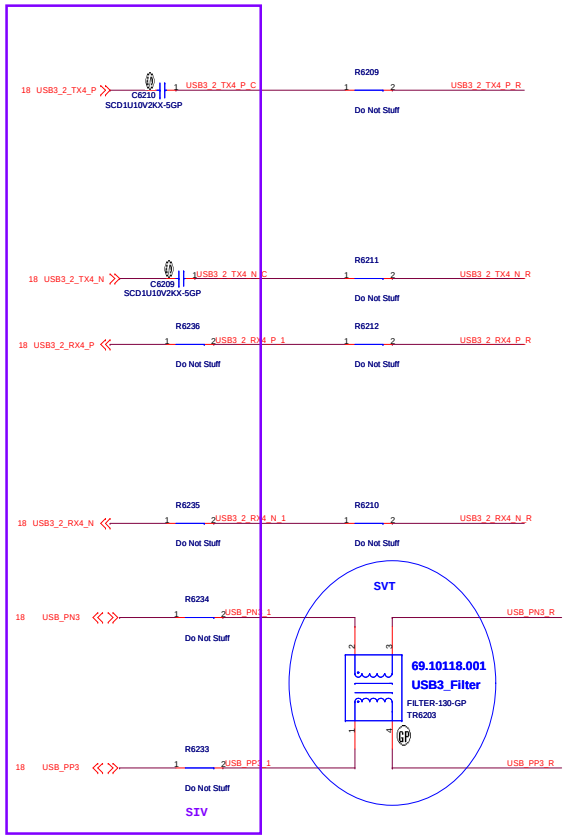
22.10339.931

2nd = 22.10339.C11

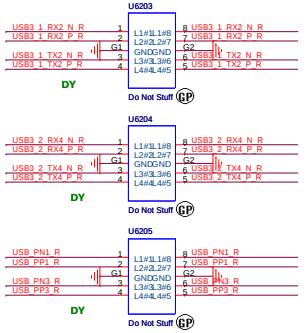
TC6202 place near
the USB2 connector

Co-Layout USB2.0 22.10321.S01





LAN surge circuit



BOM

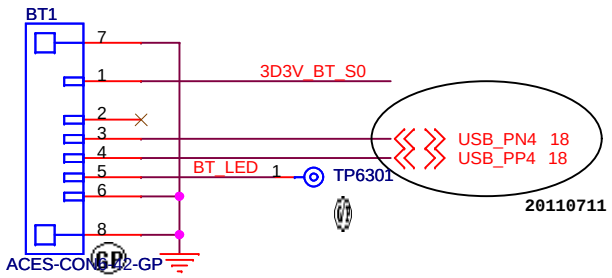
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 Port1/2	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 62 of 103	

SSID = User.Interface

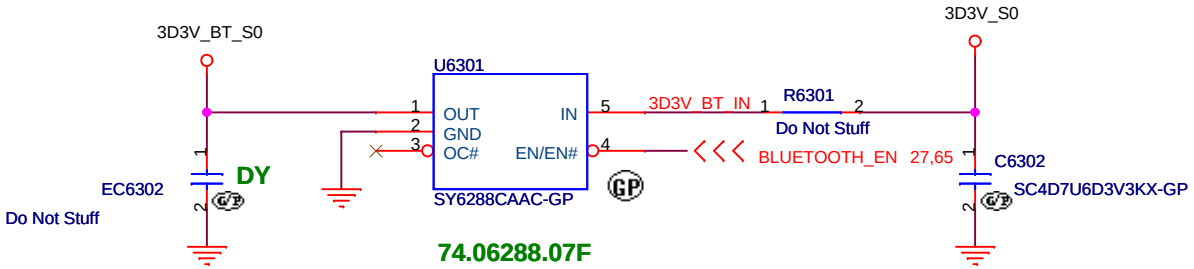
Bluetooth conn.



20.F1705.006

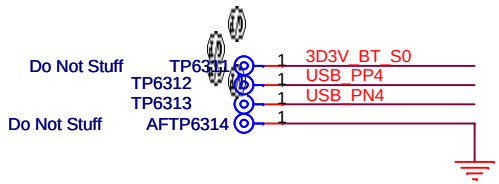
2nd = 20.F1804.006

3rd = 20.F1571.006



74.06288.07F

EC6302 put near BLUE1 / all USB put one choke near connector by EMI request

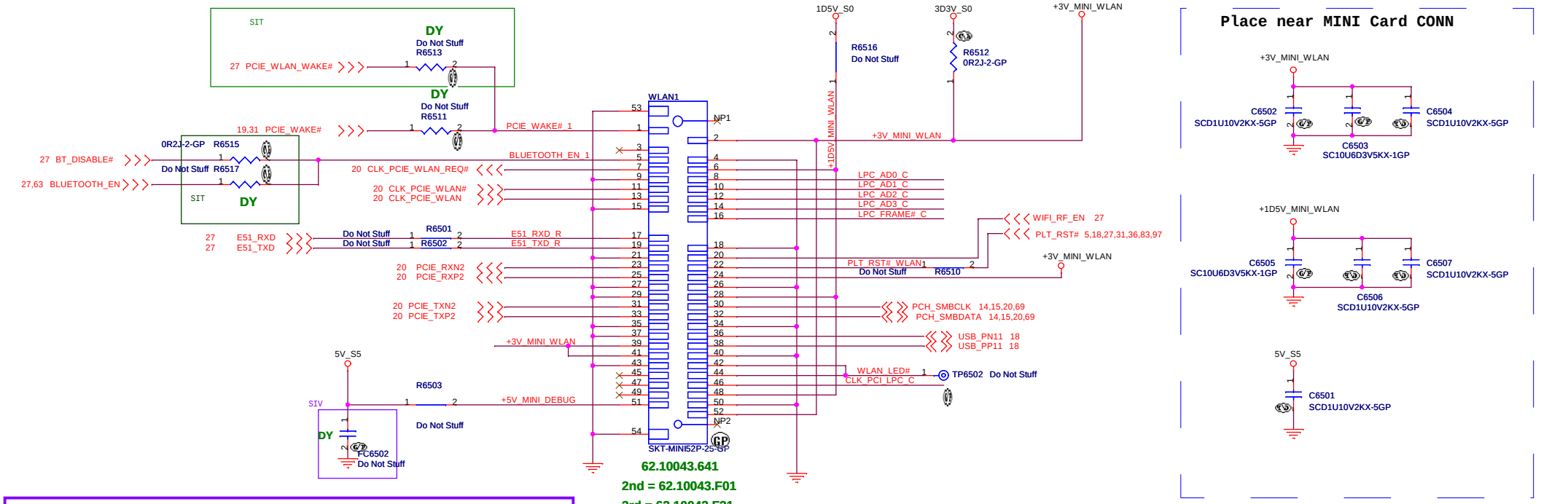


BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *BLUETOOTH*		
Size	Document Number: **LG4858L**	Rev: **SB**
Date: Friday, March 16, 2012	Sheet 63 of 103	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

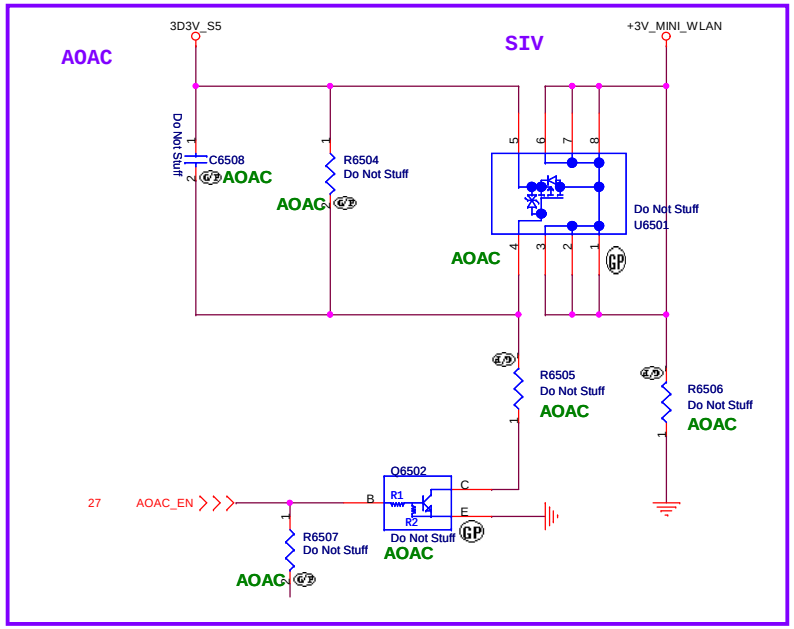


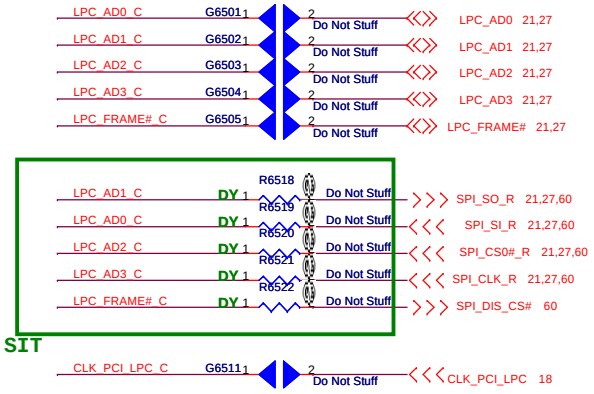
62.10043.641

2nd = 62.10043.F01

3rd = 62.10043.F21

Place near MINI Card CONN





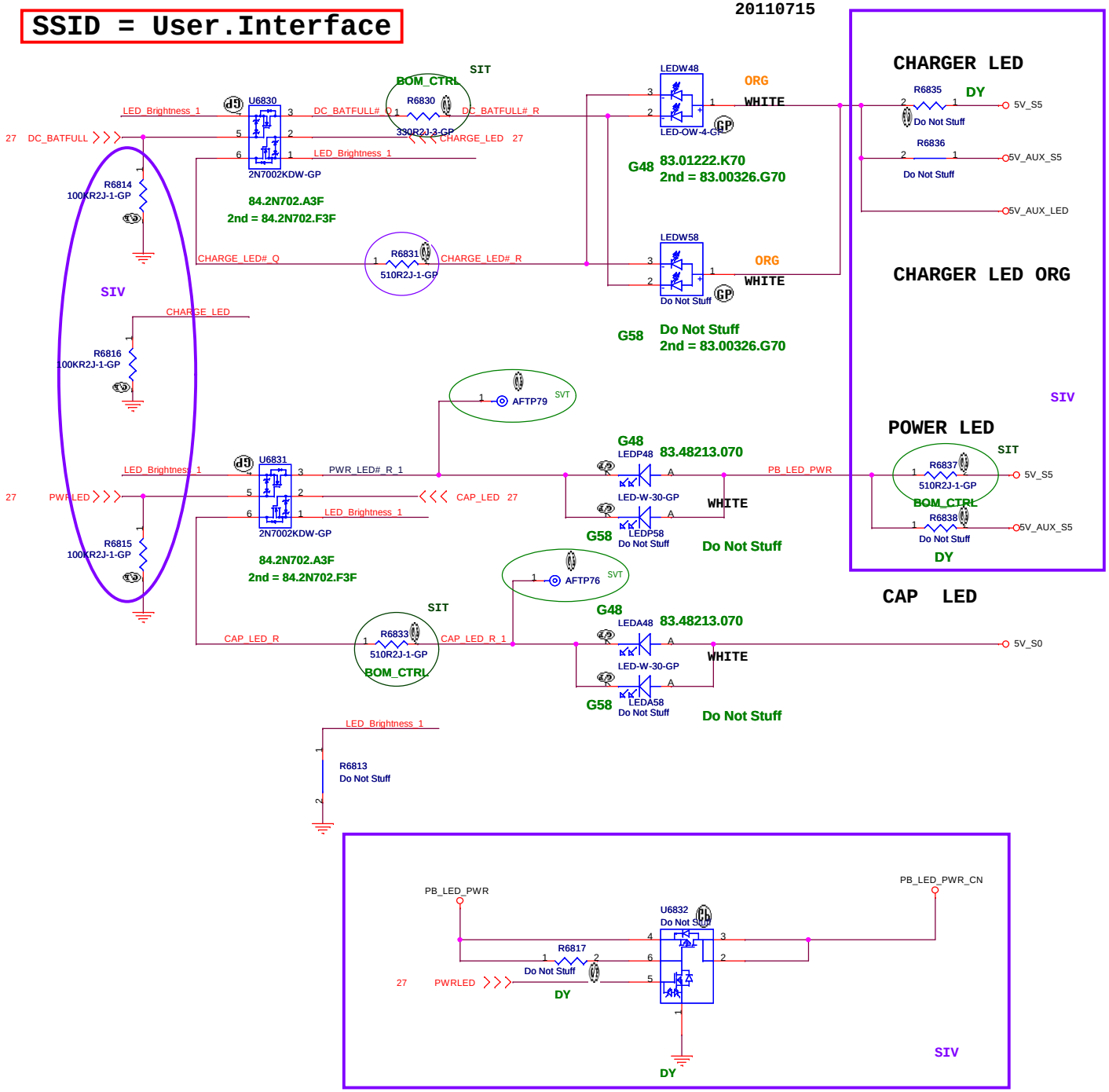
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***WLAN***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 65 of 103	

SSID = User.Interface

20110715



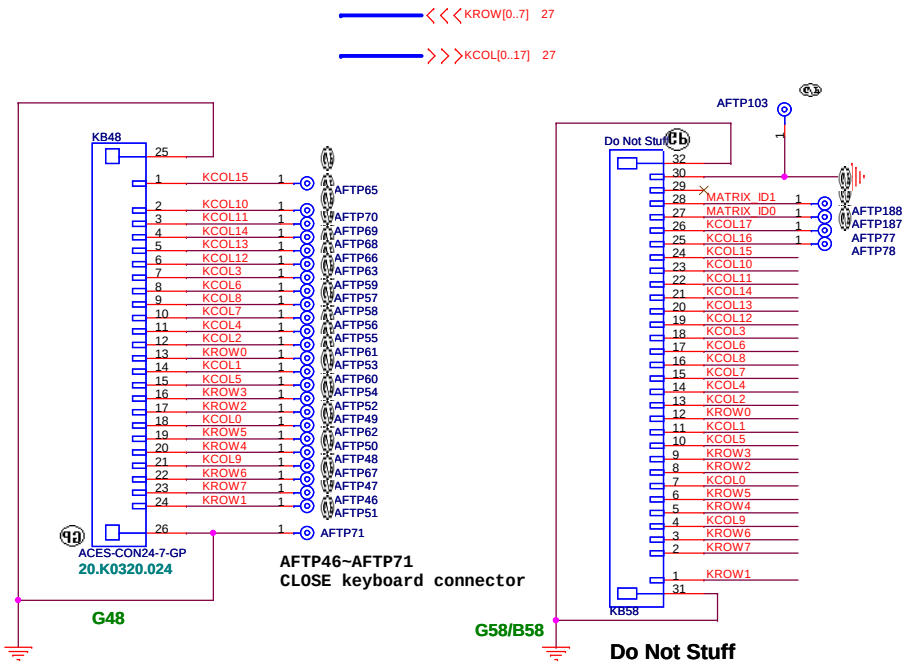
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*LED/Power Button/key*	
Size	Document Number: LG4858L	Rev: SB
Date: Friday, March 16, 2012	Sheet 68 of 103	

SSID = KBC

KB1 Follow LA47

Internal KeyBoard Connector



14"

* Membrane Pin Out Top View :

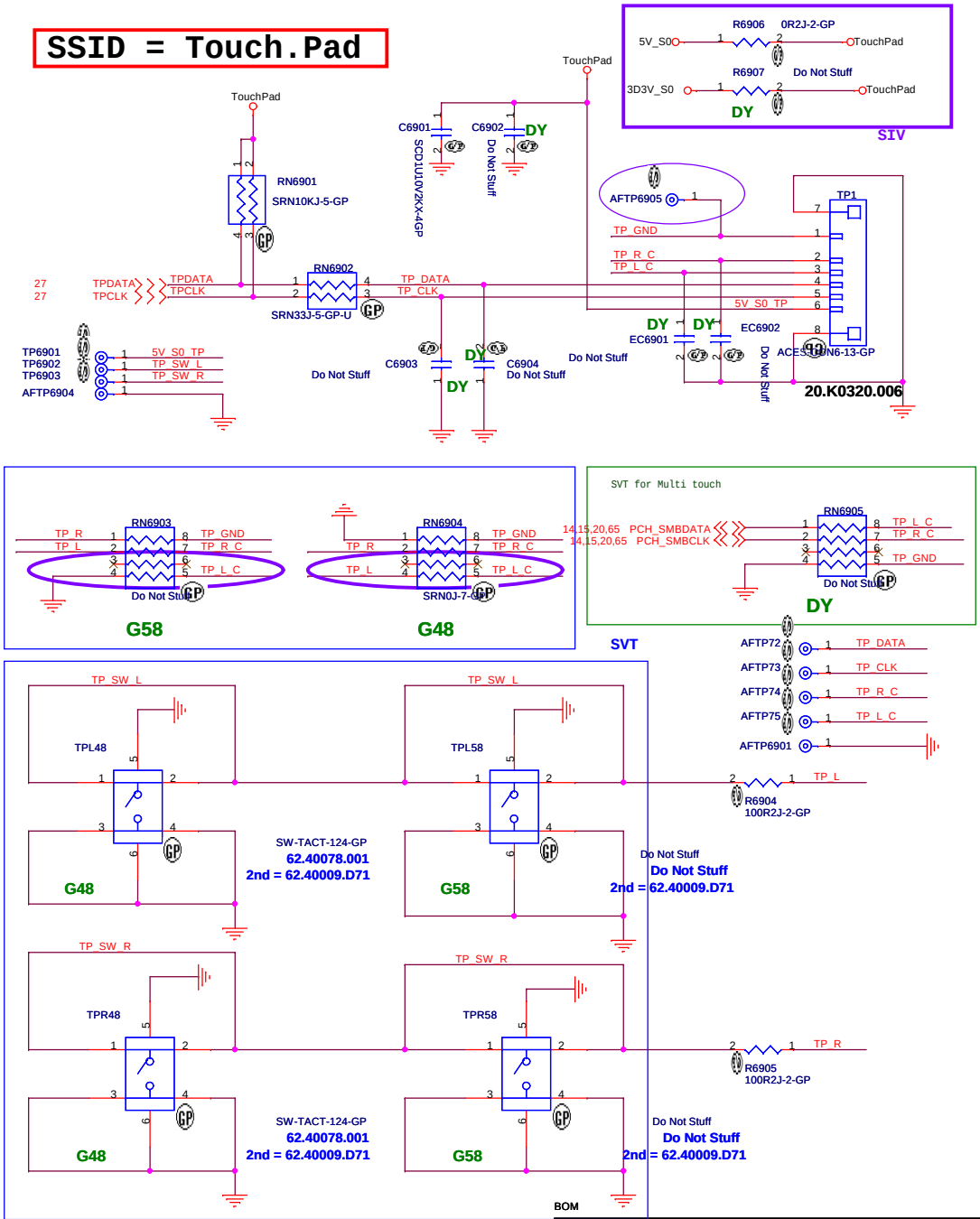
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

15"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

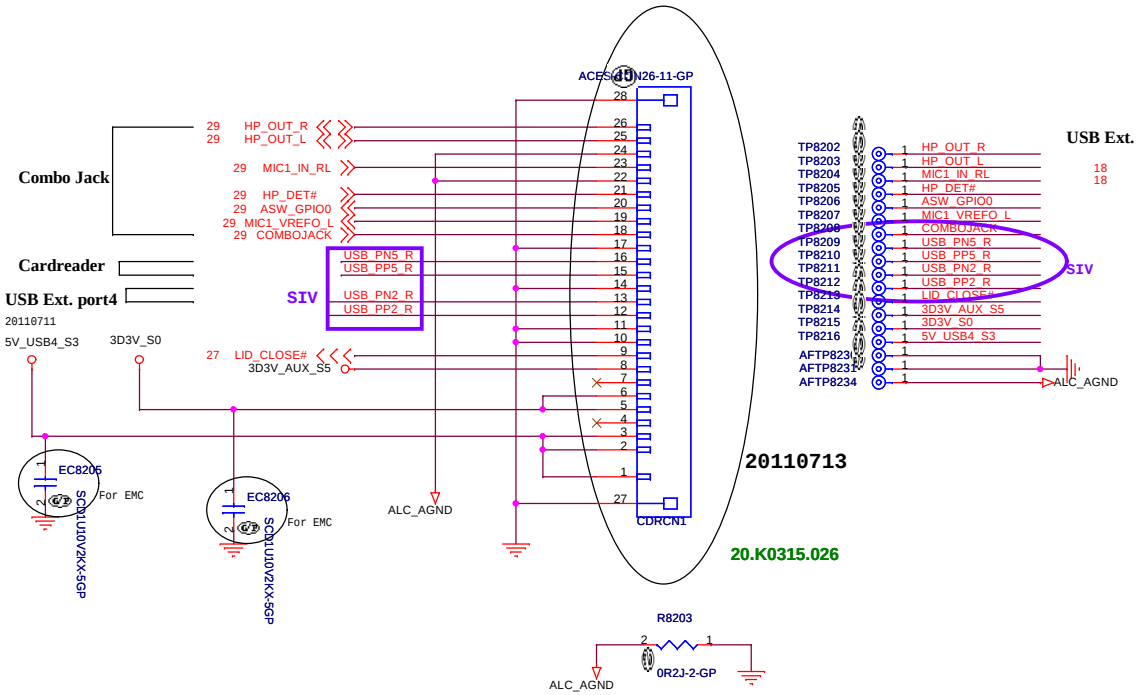
SSID = Touch.Pad



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

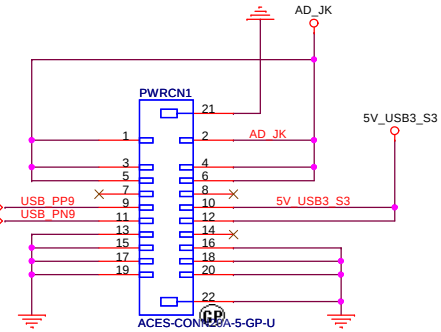
Title	Key Board/Touch Pad		
Size	Document Number	LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 69 of 103		

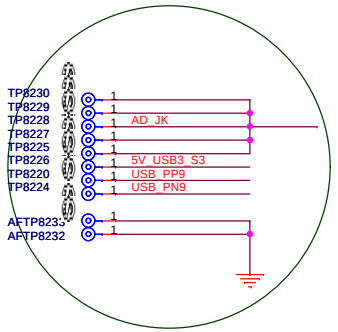
Cardreader BD connector
(Cardreader/Combo Jack/USB2.0 port4)

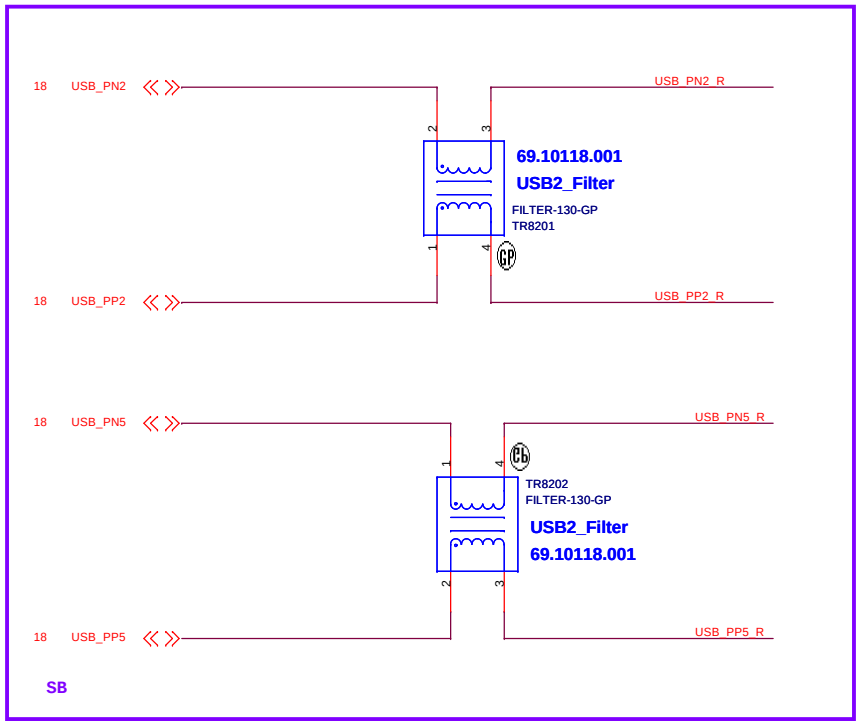


USB Ext. port3

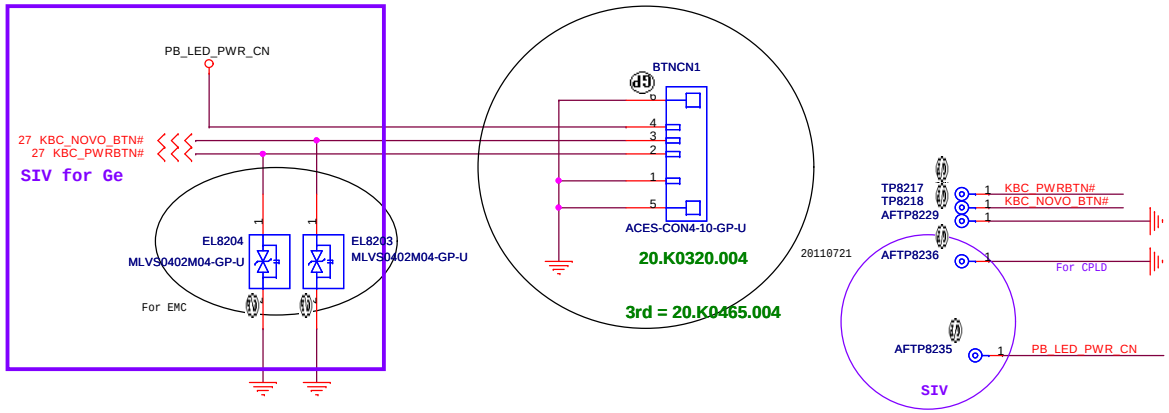
USB BD connector
(DC Jack/USB2.0 port3)





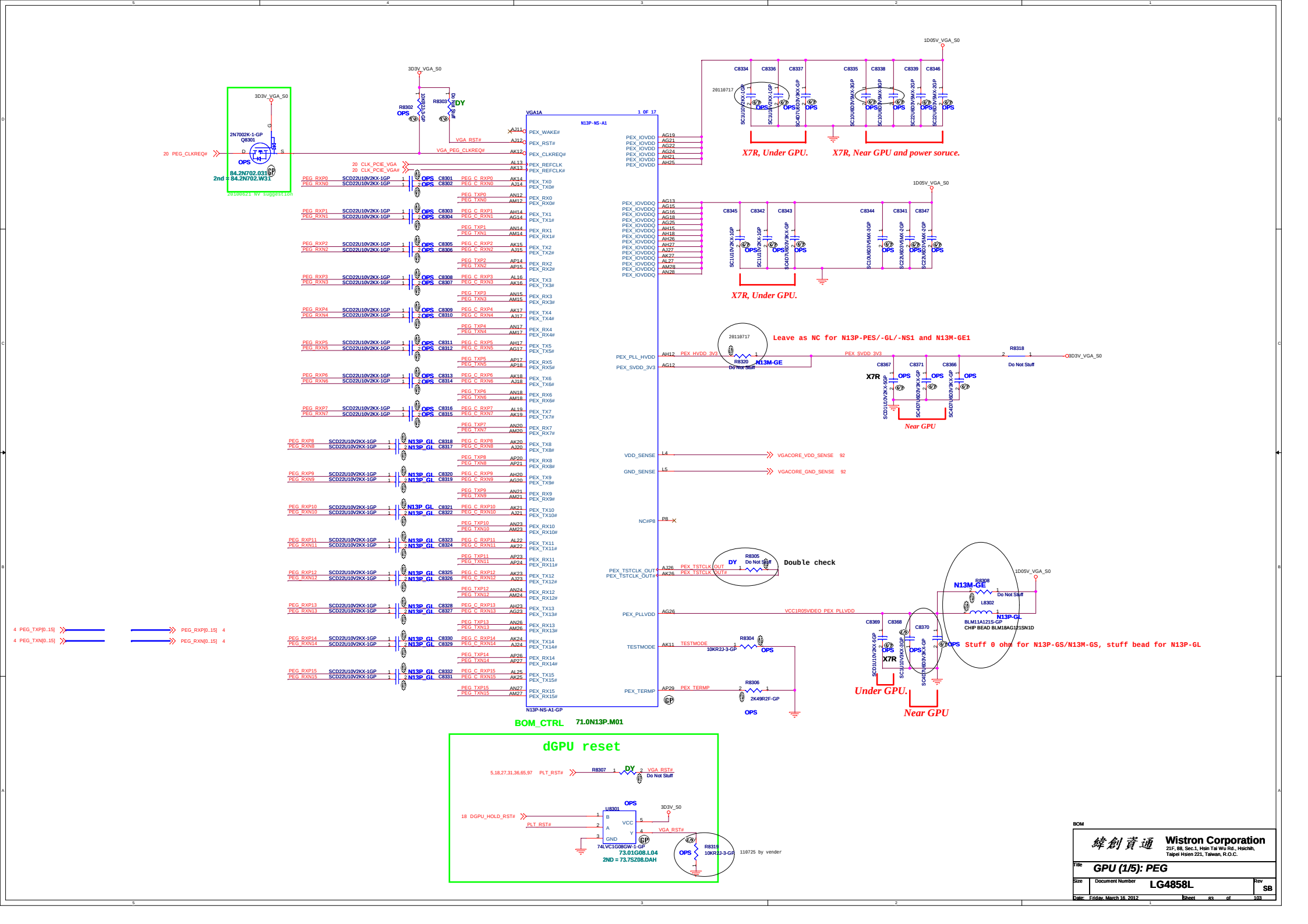


Button BD connector
(Power button/NOVO button)



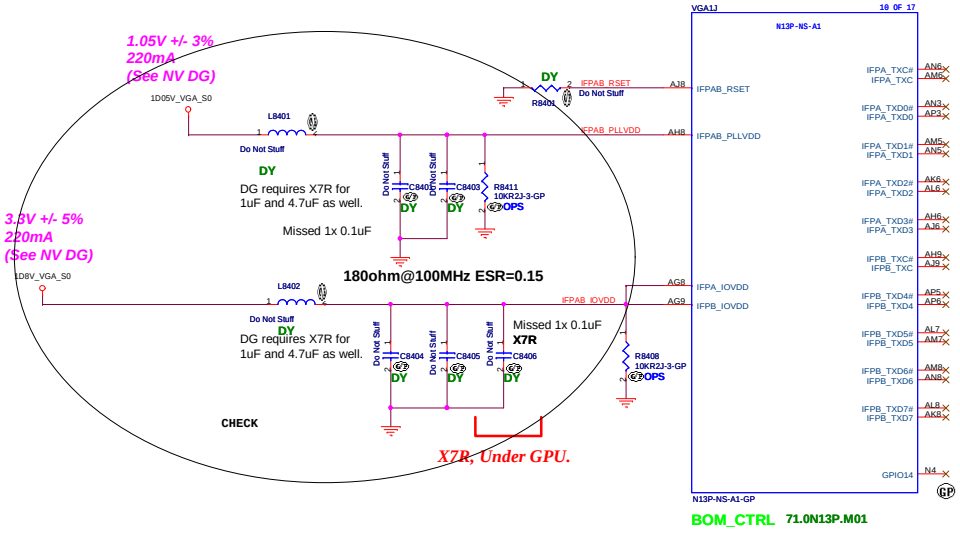
BOM

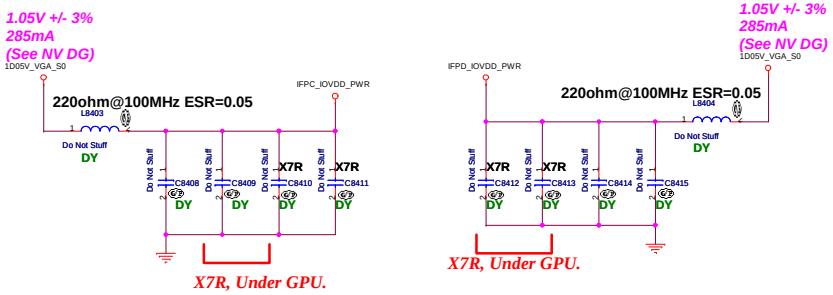
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *IO Board Connector*		
Size	Document Number: LG4858L	Rev: SB
Date: Friday, March 16, 2012	Sheet 82 of 103	

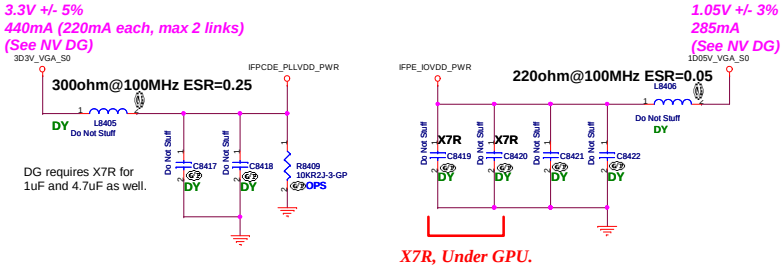

VGA_RST#
VGA_PEG_CLKREQ#
PEG_CLKREQ#
CLK_PCIE_VGA
CLK_PCIE_VGA#
VGA1A
N13P-NS-A1
1 OF 17
N13P-NS-A1-GP
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_IOVDD
PEX_IOVDDQ
PEX_PLL_HVDD
PEX_SVDD_3V3
VDD_SENSE
GND_SENSE
NC#P8
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_PLLVDD
TESTMODE
PEX_TERMP
PEG_RXP[0..15]
PEG_RXN[0..15]
PEG_TXP[0..15]
PEG_TXN[0..15]
VGACORE_VDD_SENSE
VGACORE_GND_SENSE
Leave as NC for N13P-PES/-GL/-NS1 and N13M-GE1
X7R, Under GPU.
X7R, Near GPU and power soruce.
Near GPU
Double check
Under GPU.
Stuff 0 ohm for N13P-GS/N13M-GS, stuff bead for N13P-GL
BOM_CTRL
71.0N13P.M01
dGPU reset
DGPU_HOLD_RST#
Wistron Corporation
GPU (1/5): PEG
LG4858L

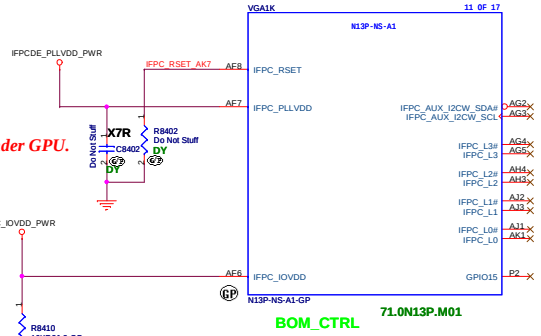
RD480_SA:71.0N12P.M08

LVDS Interface

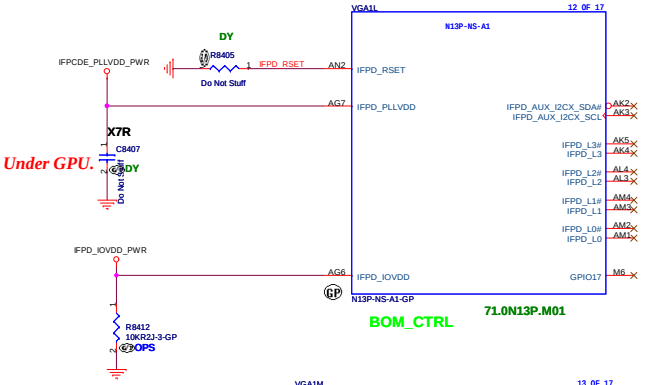


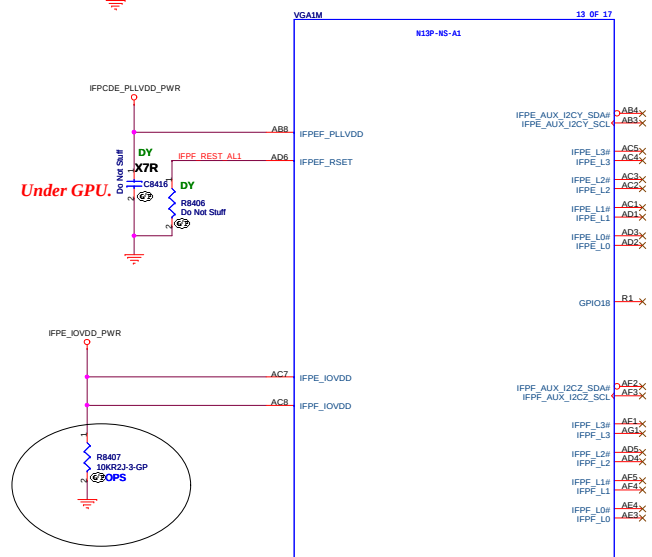






HDMI Interface

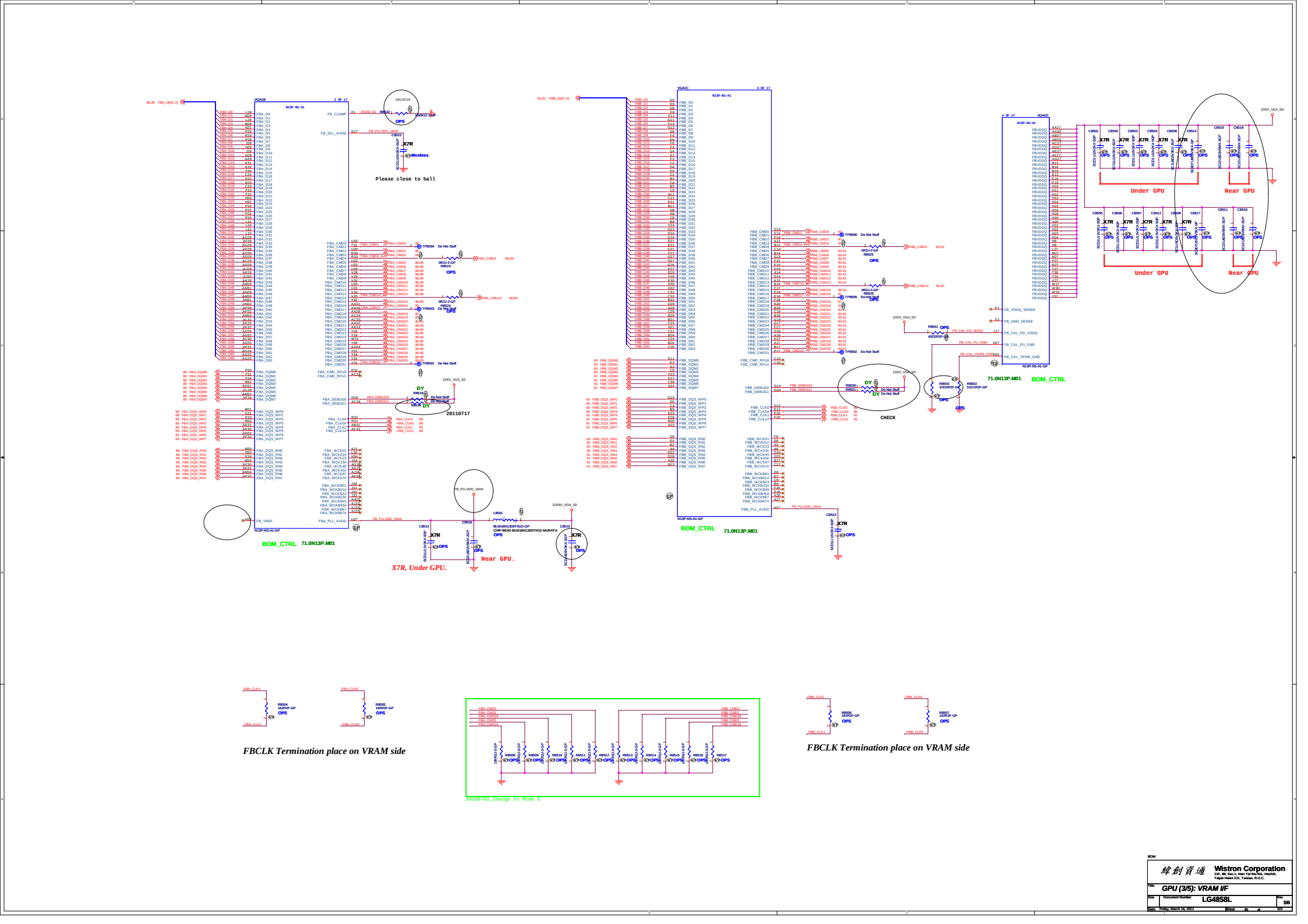




BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

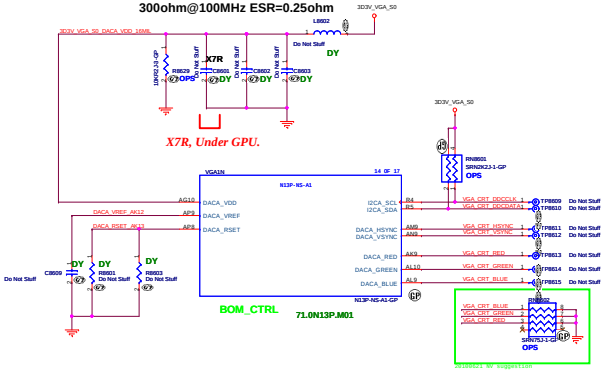
Title	GPU (2/5): DIGITALOUT	
Size	Document Number LG4858L	Rev SB
Date: Friday, March 16, 2012	Sheet 84 of 103	

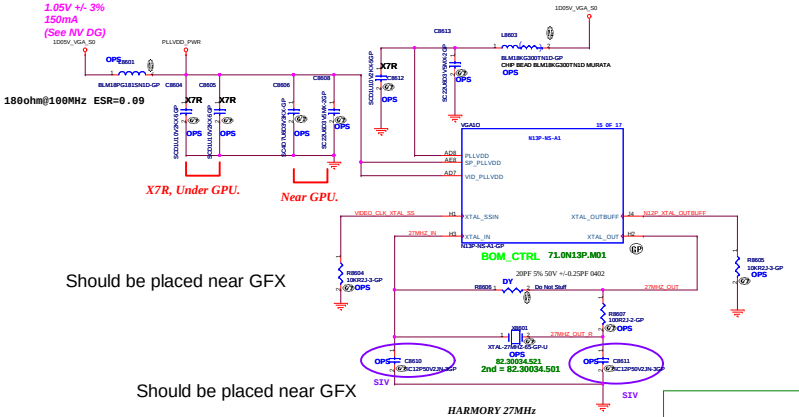


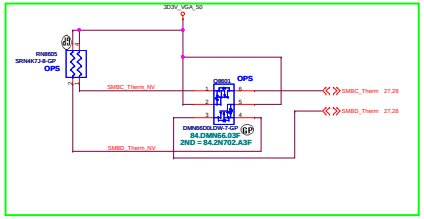
BOM

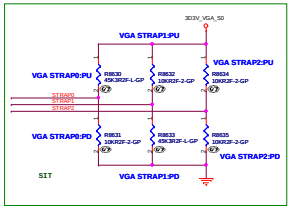
緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU (3/5): VRAM I/F	
Size	Document Number: LG4858L	Rev: SB
Date: Friday, March 16, 2012	Sheet: 85 of 103	

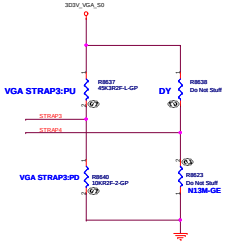
RD480_SA:71.0N12P.M08











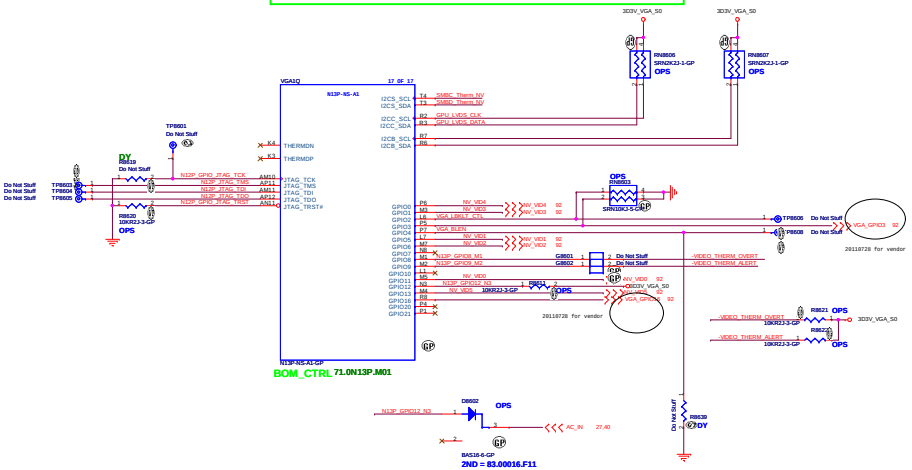
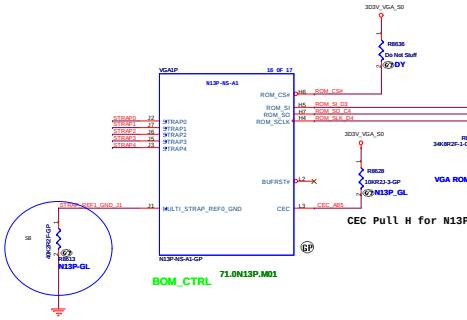


	TABLE NVIDIA	N13P-GL(PS) DEV ID: 0x0DE9
STRAP0	R8630(PU)	45.3Kohm 64.45325.6DL
	R8631(PD)	DY
STRAP1	R8632(PU)	DY
	R8633(PD)	45.3Kohm 64.45325.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL
	R8635(PD)	DY
STRAP3	R8637(PU)	DY
	R8640(PD)	DY
STRAP4	R8638(PU)	DY
	R8623(PD)	DY

	TABLE NVIDIA	N13M-GE(PS) Old SAMSUNG 128Mx16 72.42164.D0U	New SAMSUNG 128Mx16 72.42164.G0U	Old HYNIX 128Mx16 72.52G63.A0U	New HYNIX 128Mx16 72.52G63.C0U	Samsung 64Mx16	HYNIX 64Mx16
STRAP0	R8630(PU)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	DY	10Kohm 64.10025.6DL	DY
	R8631(PD)	DY	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP1	R8632(PU)	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8633(PD)	10Kohm 64.10025.6DL	DY	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
	R8635(PD)	DY	10Kohm 64.10025.6DL	DY	DY	10Kohm 64.10025.6DL	DY
STRAP3	R8637(PU)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	DY
	R8640(PD)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
STRAP4	R8638(PU)	DY	DY	DY	DY	DY	DY
	R8623(PD)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL



VGA	N13P-GL(PS) 71.0N13P.E0U	N13M-GE(PS) 71.0N13M.B1U
ROM_SO PD R8617	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
ROM_SCLK PD R8618	15Kohm 64.15025.6DL	10Kohm 64.10025.6DL

TABLE
VIDEO MEMORY

Nvidia VGA	900MHz	Old HYNIX 128Mx16 72.52G63.A0U	New HYNIX 128Mx16 72.52G63.C0U	SAMSUNG 128Mx16 72.42164.D0U 72.42164.G0U	HYNIX 64Mx16 72.51G63.H0U	Samsung 64Mx16 72.41646.Q0U
N13P-GL	ROM_SI PD R8627	34.8K ohm 64.34825.6DL	30.1K ohm 64.30125.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL
N13M-GE	ROM_SI PD R8627	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL

Wistron Corporation
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Title: GPU (4/5): GPIO/STRAP

Size: Document Number: LG4858L Rev: SB

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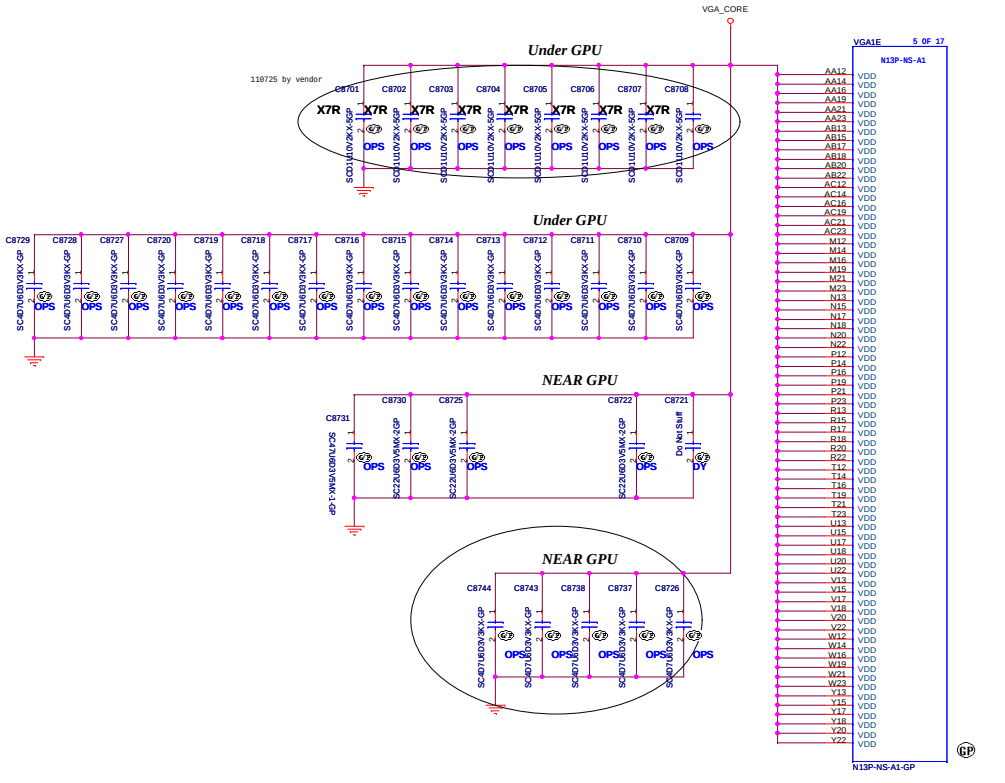

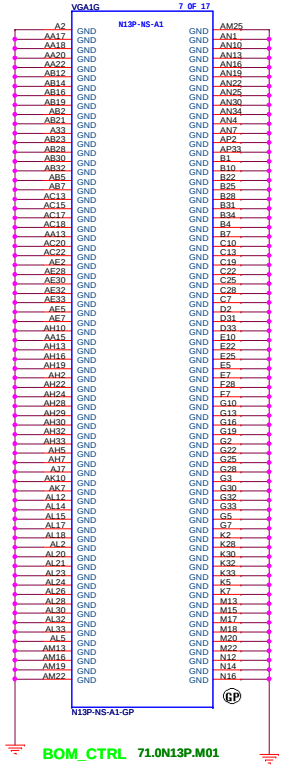

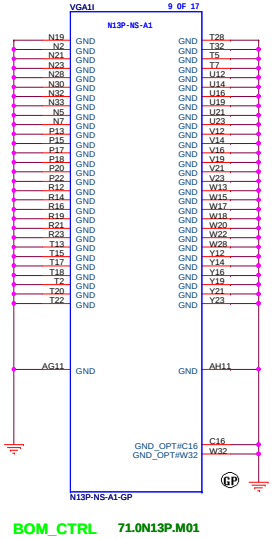

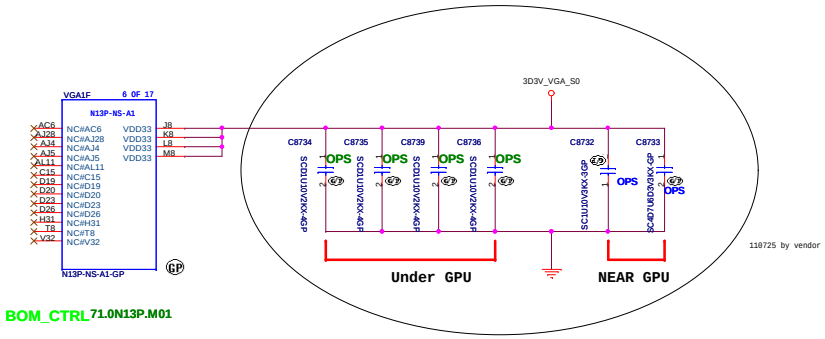

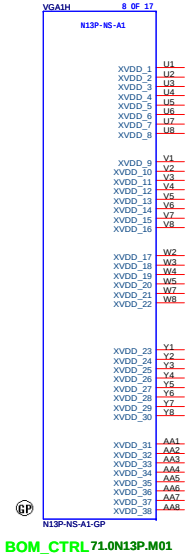

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (5/5): PWR/GND	
Size	Document Number LG4858L	Rev SB
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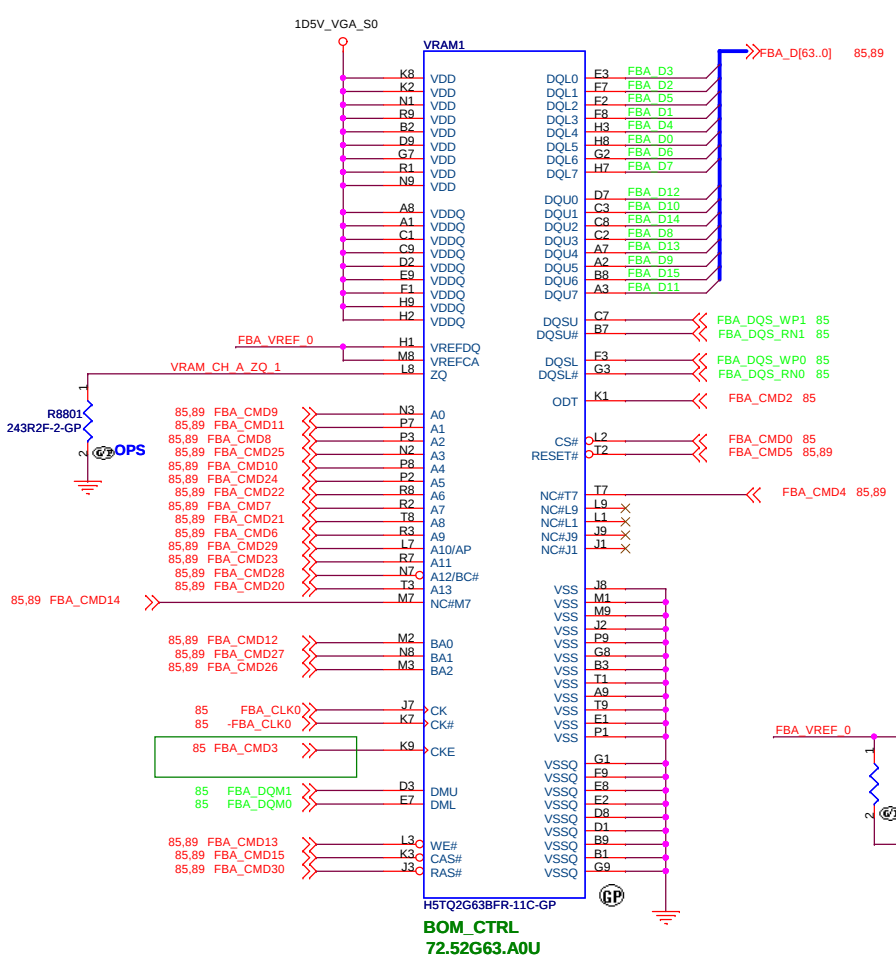
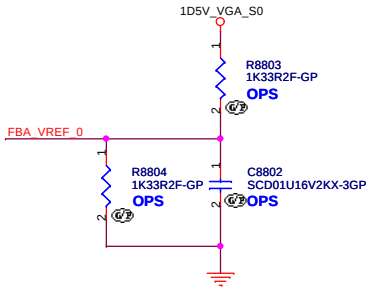
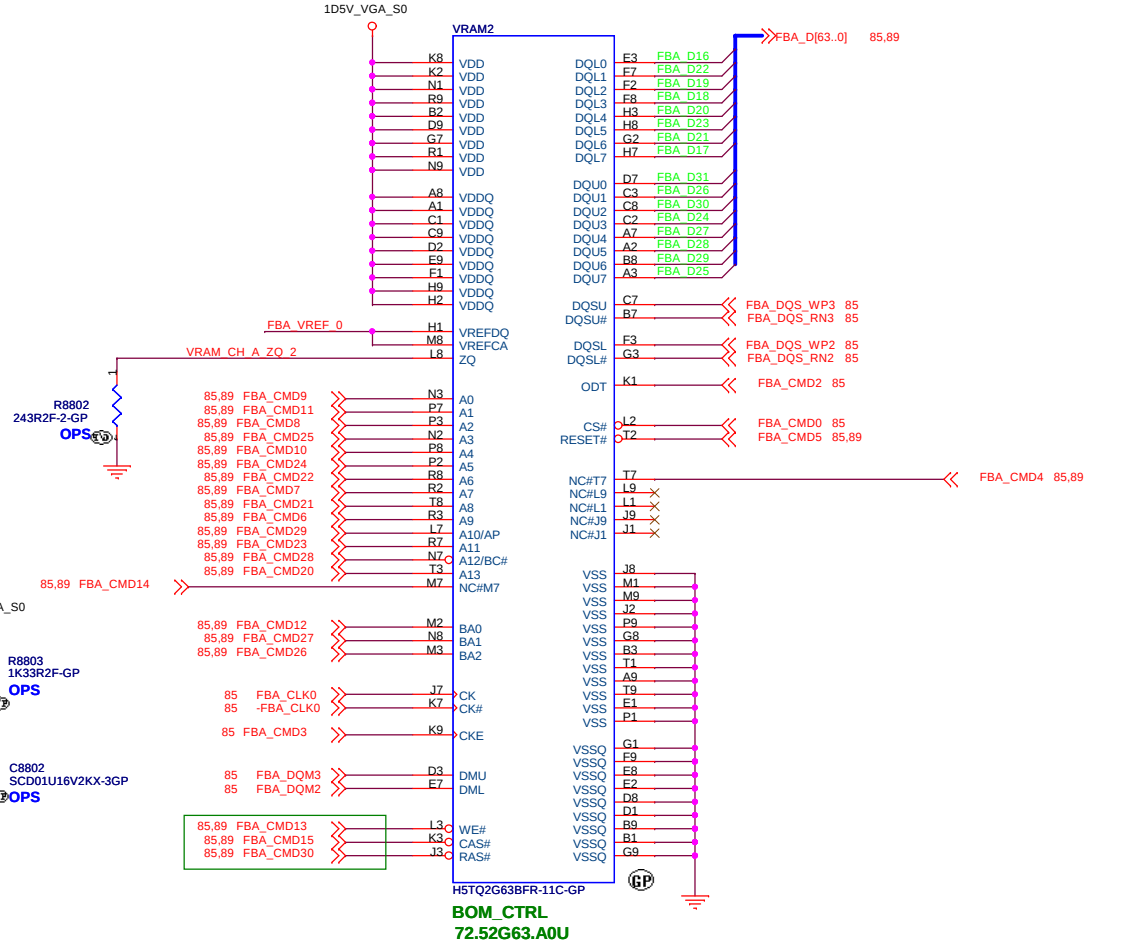
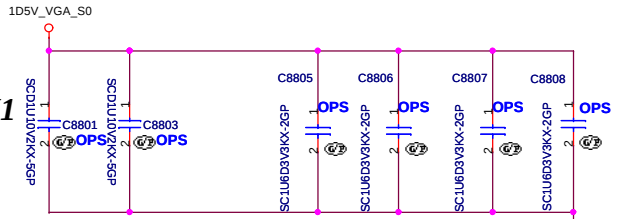


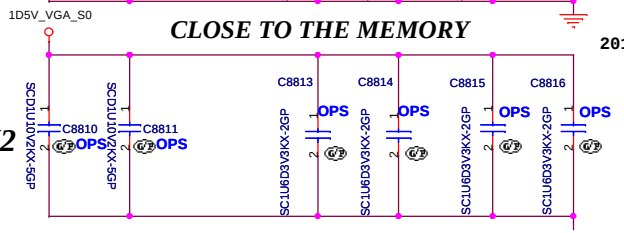






FOR VRAM1

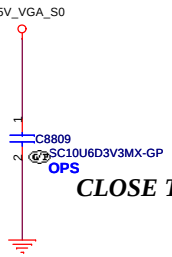
CLOSE TO THE MEMORY



FOR VRAM2

20110725 for Vendor

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

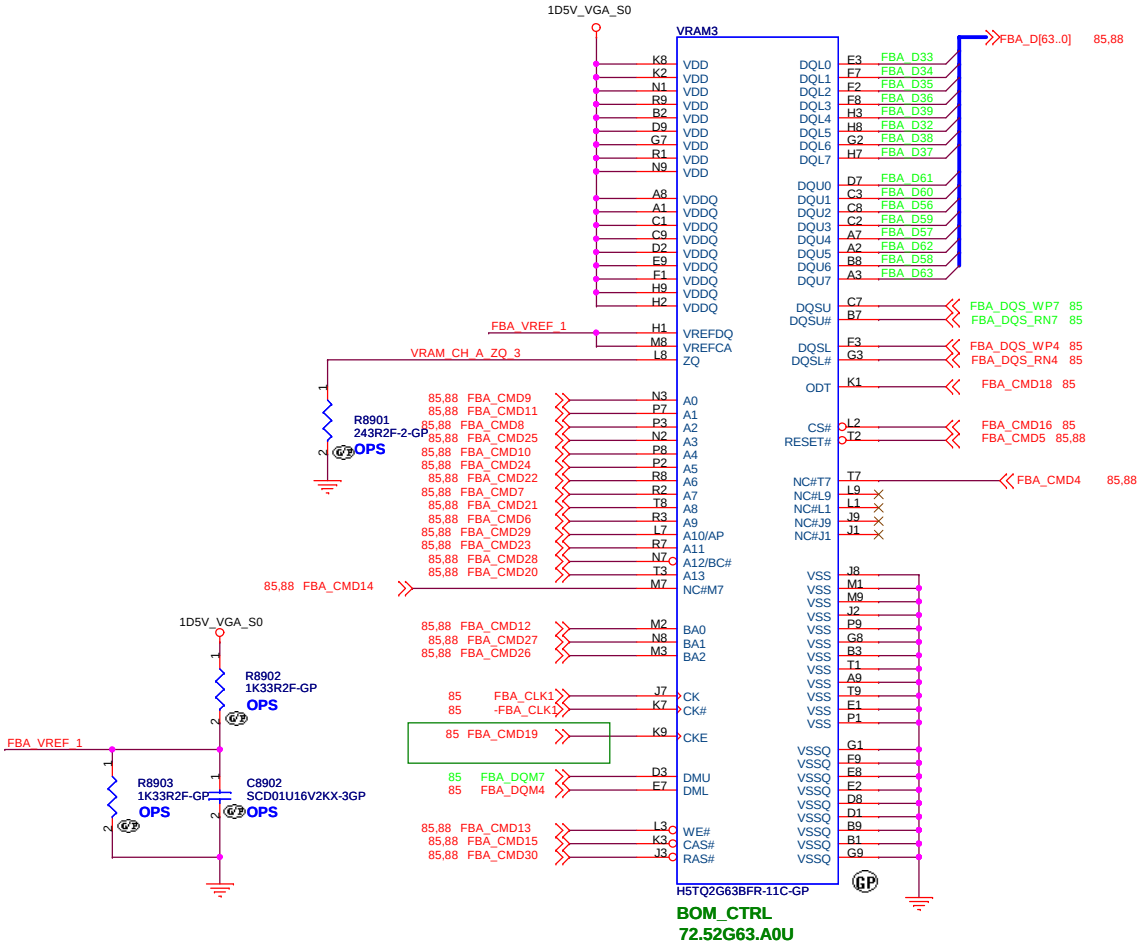
HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

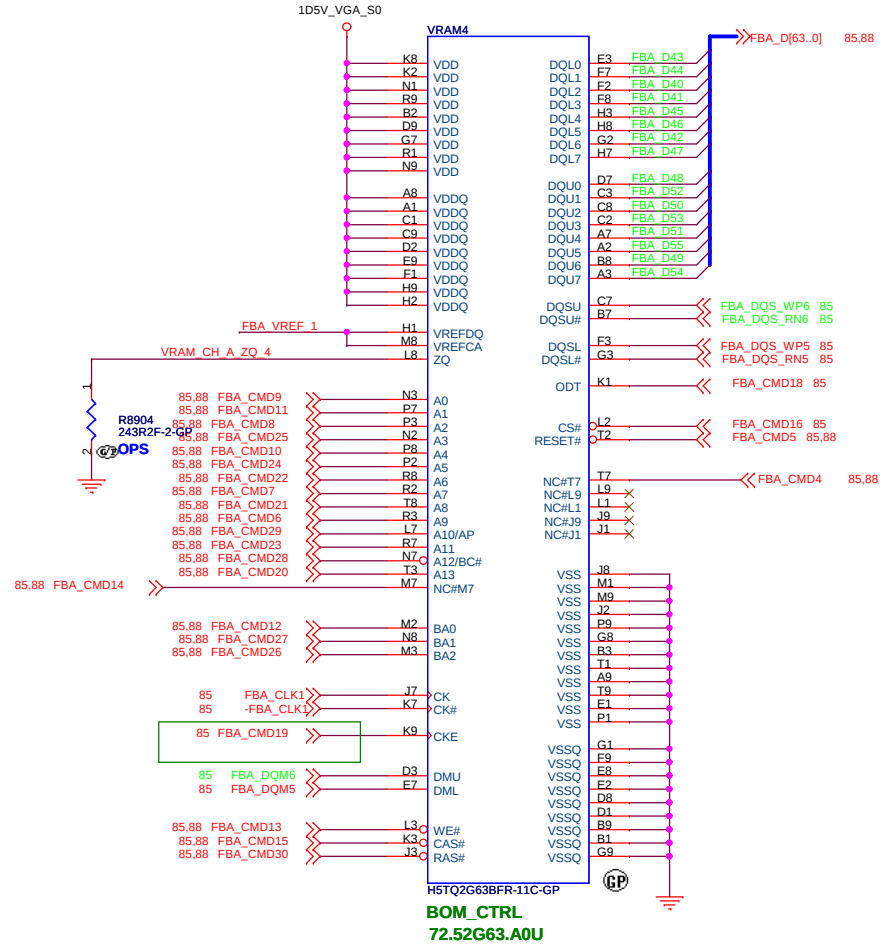
VIDEO FRAME BUFFER PORT A

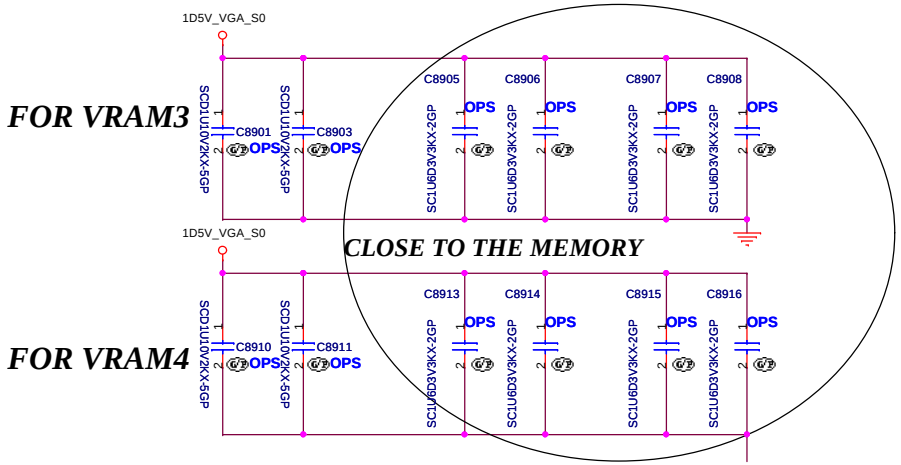
BOM

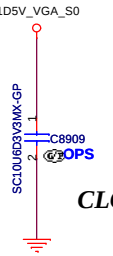
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VRAM1,2 (1/4)***	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 88 of 103	









VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

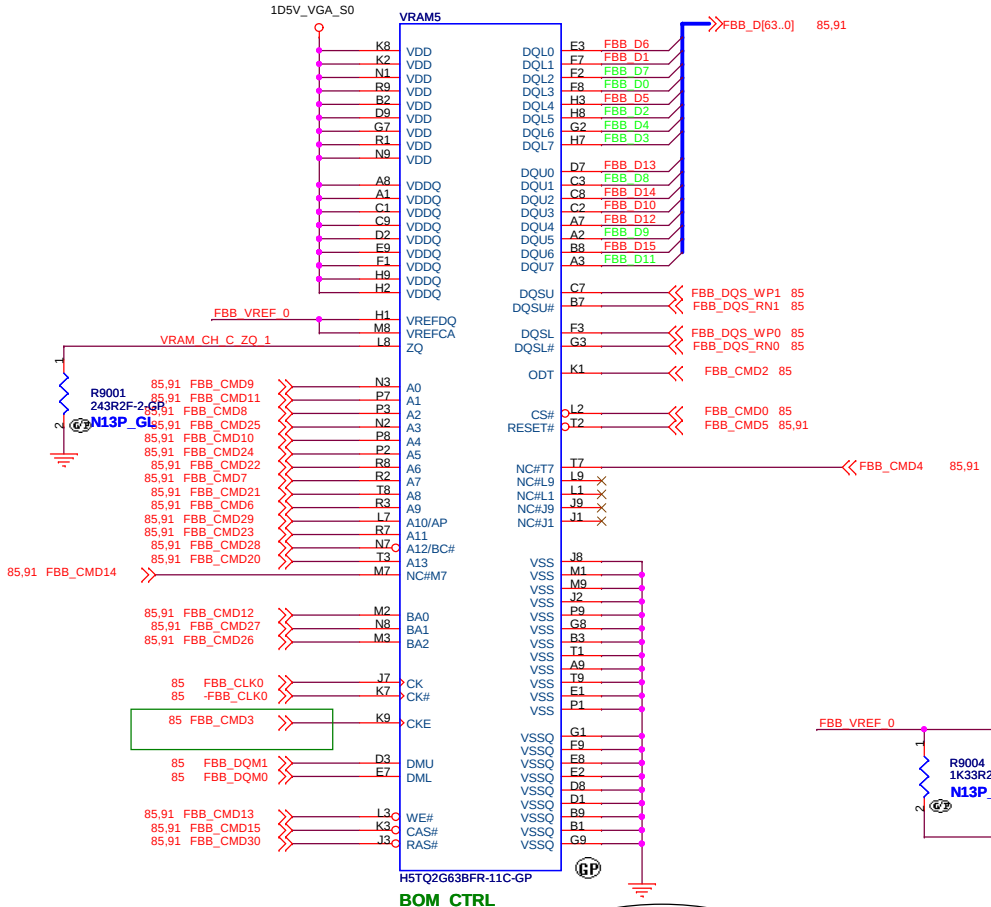
HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

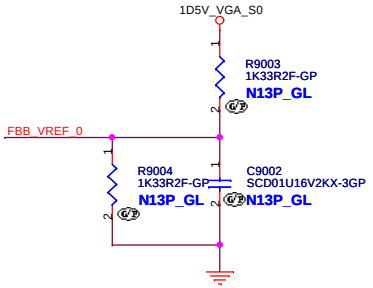
VIDEO FRAME BUFFER PORT A

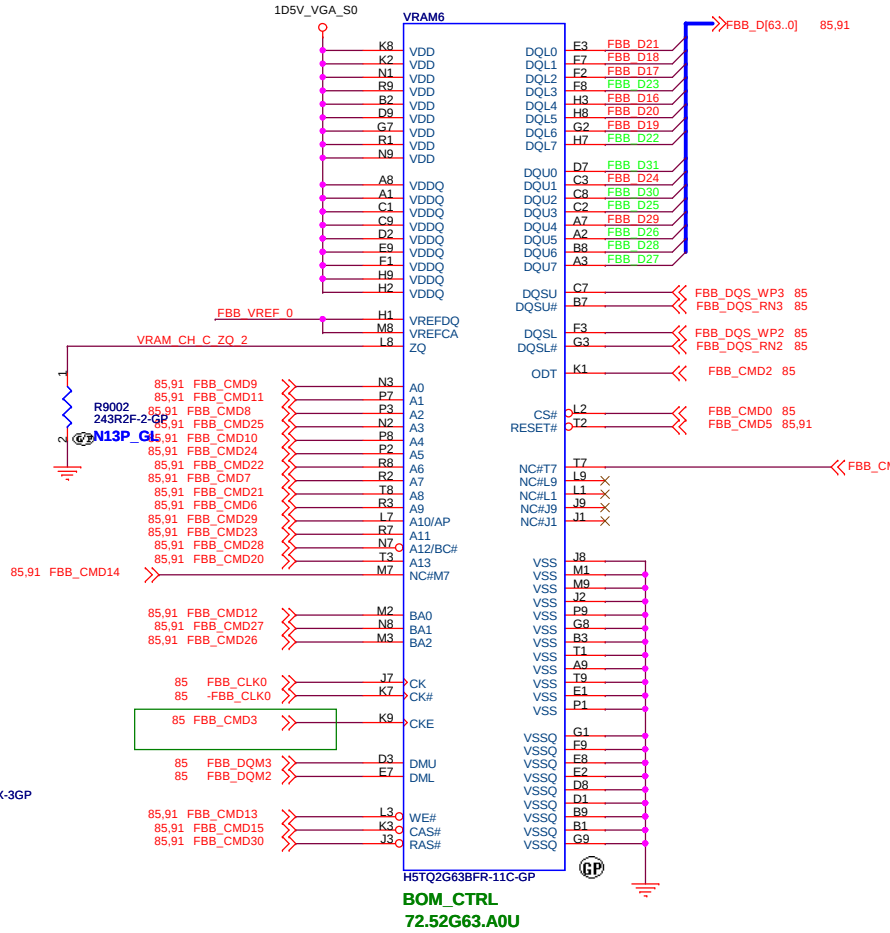
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

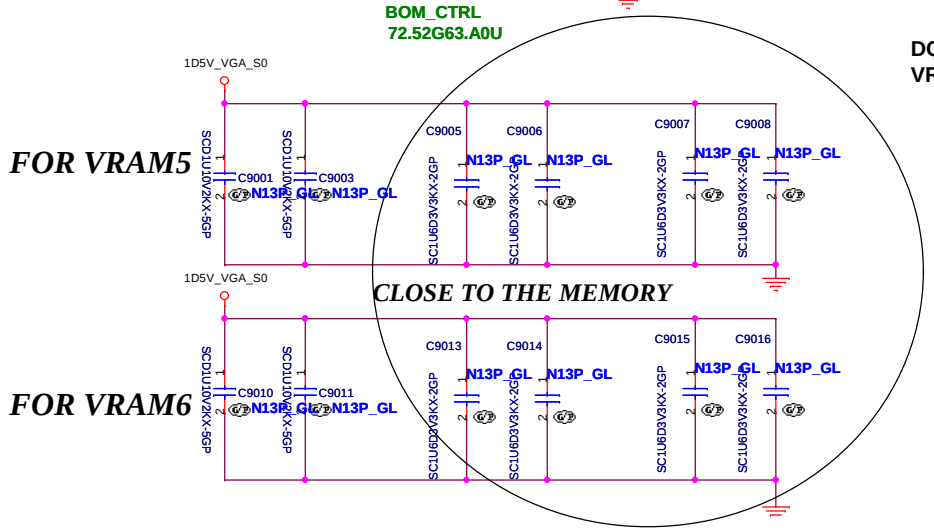
Title	***VRAM3,4 (2/4)***		
Size	Document Number **LG4858L**		Rev **SB**
Date: Friday, March 16, 2012	Sheet 89 of 103		

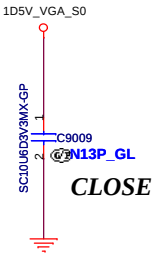






DG requires 4x0.1uF and 8x1.0uF per VRAM chip





VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

BOM *VIDEO FRAME BUFFER PORT C*

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VRAM5,6 (3/4)***	
Size	Document Number **LG4858L**	Rev **SB**
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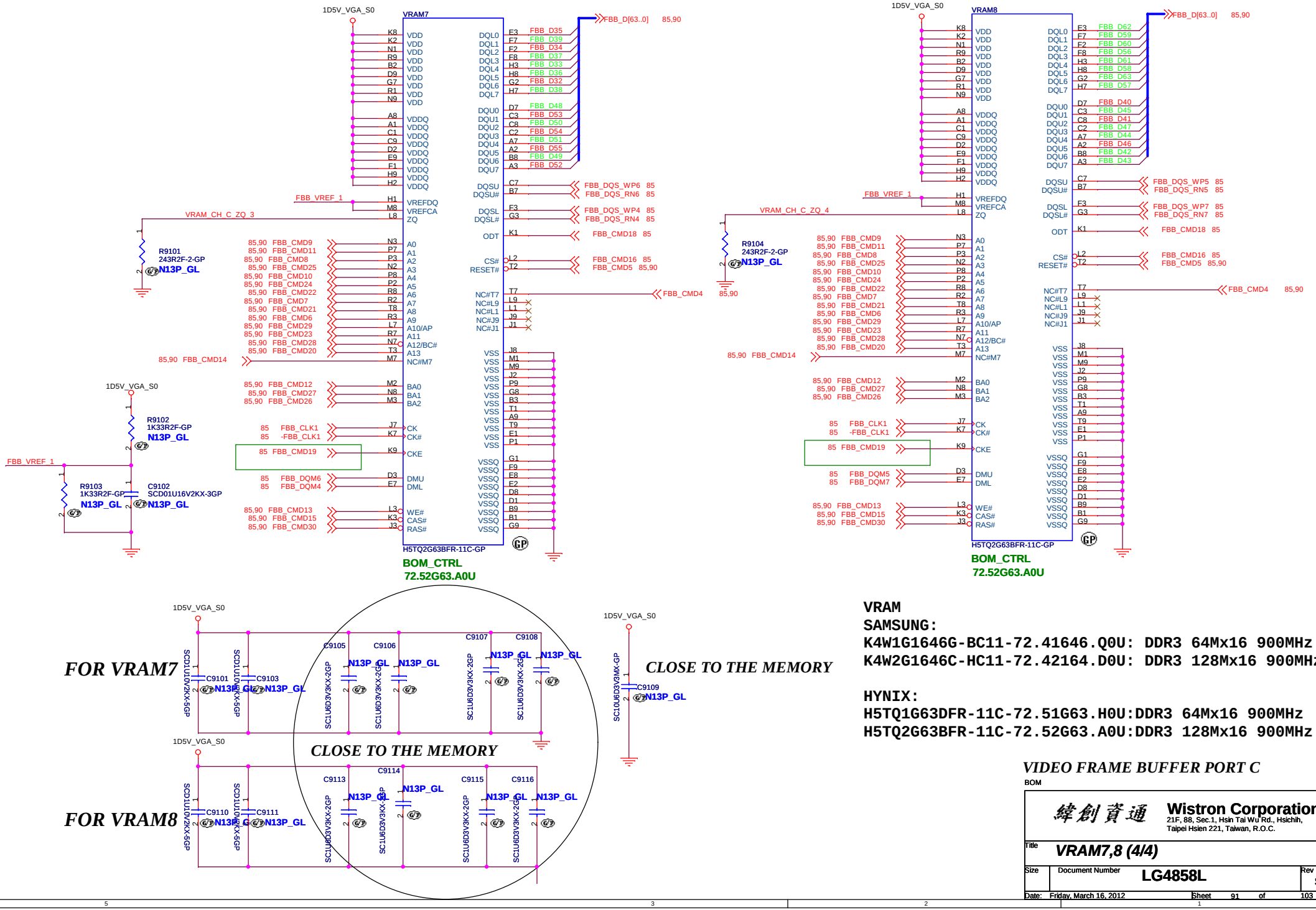


VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT C

BOM

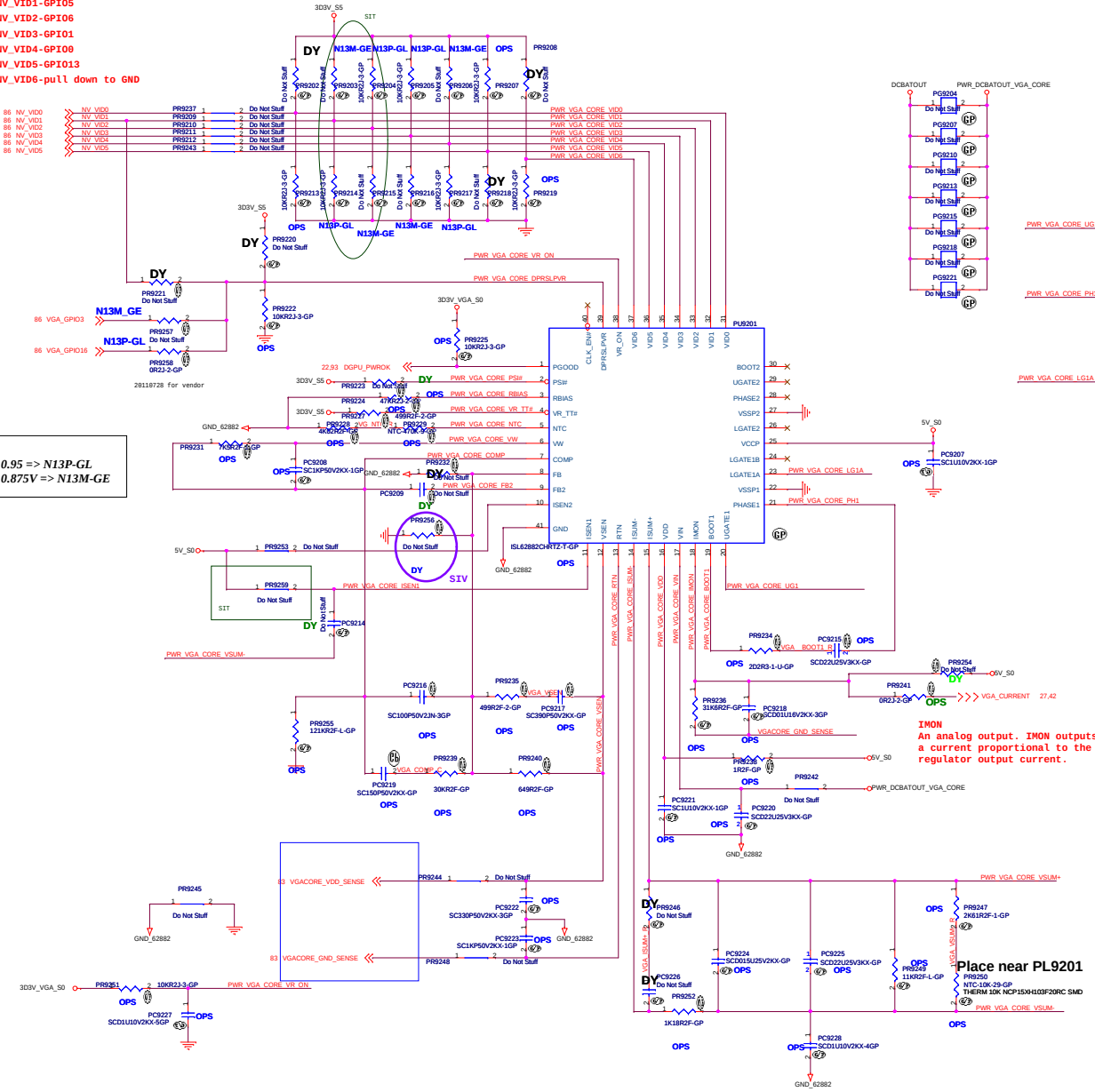
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM7,8 (4/4)*	
Size	Document Number **LG4858L**	Rev **SB**
Date: Friday, March 16, 2012	Sheet 91 of 103	

SSID = PWR.Plane.Regulator_VGACORE

NV_VID0-GPIO11
NV_VID1-GPIO5
NV_VID2-GPIO6
NV_VID3-GPIO1
NV_VID4-GPIO0
NV_VID5-GPIO13
NV_VID6-pull down to GND

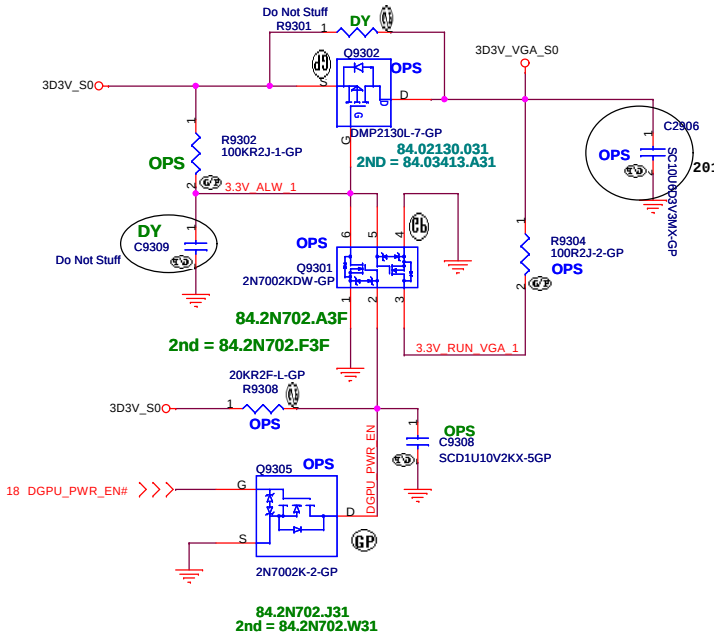
VID[5..0]
101100 = 0.95 => N13P-GL
110010 = 0.875V => N13M-GE



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL62882C_GPU_CORE
Size	Document Number: LG4858L — Rev: SB
Date: Friday, March 16, 2012	Sheet 92 of 103

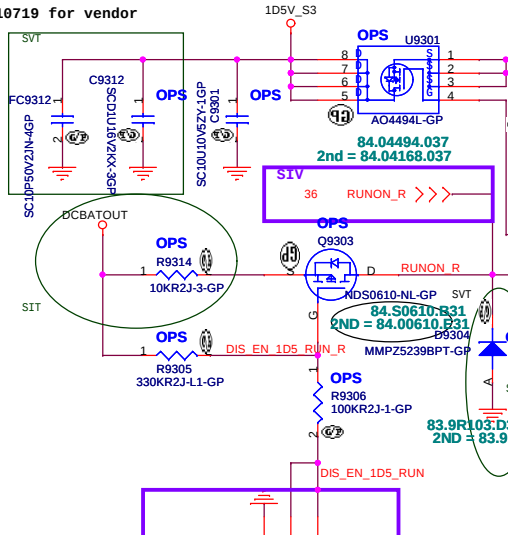
+3VS to 3.3V_DELAY Transfer

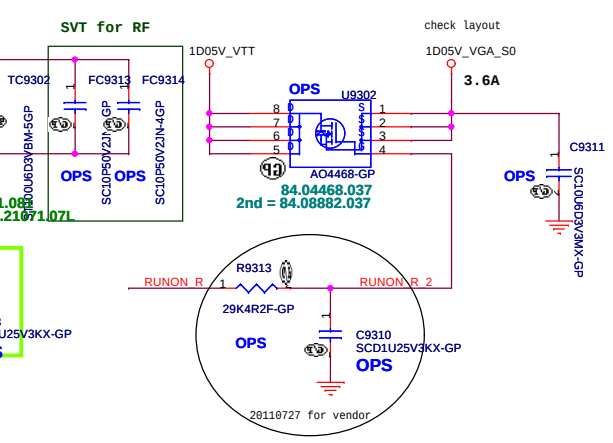


AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

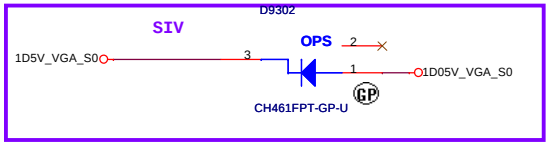
20110719 for vendor

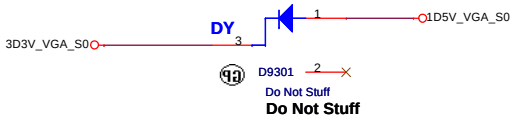
1D5V_VGA_S0





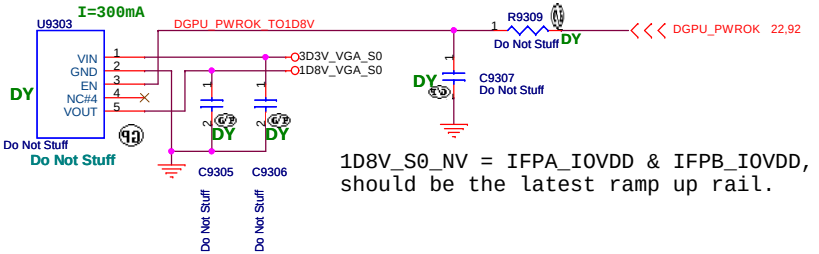
1.05V to 1.05V_VGA_S0 Transfer



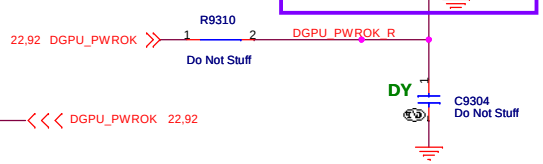


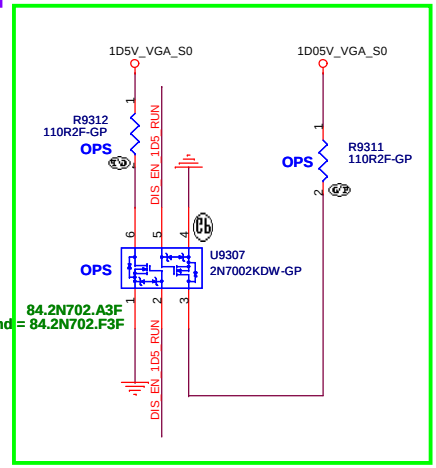
20110727 for vendor

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.





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CPU Plate

H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff

DY DY DY

VGA Std-Off

H2 STF237R128H42-GP
H1 STF237R128H42-GP

34.4GD01.101
2nd = 34.4GD01.001
OPS

34.4GD01.101
2nd = 34.4GD01.001
OPS

Check test point

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
19,27 PM_PWRBTN#	AFTP10
5,22,36 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12
5,18,27,31,36,65,83 PLT_RST#	AFTP13

Structure boss

SIT
H6 Do Not Stuff
DY
Do Not Stuff

H8 Do Not Stuff
DY
Do Not Stuff

H9 Do Not Stuff
DY
Do Not Stuff

LG4858L-SB

H10 Do Not Stuff
DY
Do Not Stuff

H11 Do Not Stuff
DY
Do Not Stuff

H13 Do Not Stuff
DY
Do Not Stuff

H14 Do Not Stuff
DY
Do Not Stuff

Spring

H16 SPRING-24-GP-U
H17 SPRING-24-GP-U
H18 SPRING-24-GP-U

SIT
H19 SPRING-52-GP
H22 SPRING-12-GP-U1

Washer

H20 Do Not Stuff
G48_PLED

H21 Do Not Stuff
G58_PLED

SIV

EMI Cap.

DCBATOUT

EC9719 EC9718 EC9717 EC9716 EC9715 EC9714 EC9713 EC9712 EC9711
SCD1U50V3KX-GP

DCBATOUT
EC9705
DY
Do Not Stuff

AD+
EC9709 EC9708
SCD1U50V3KX-GP

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Title	UNUSED PARTS/EMI Capacitors	
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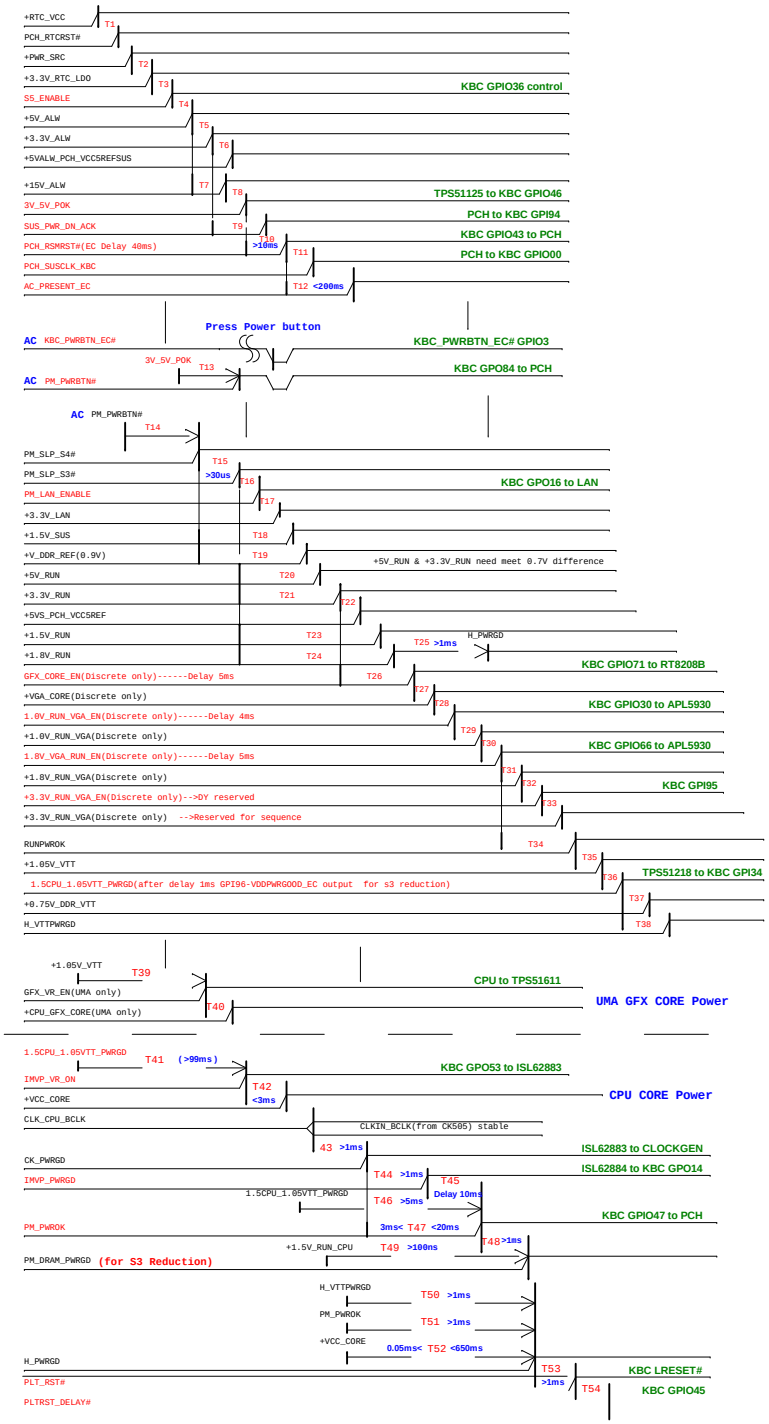
Intel-Power Up Sequence

Not Update

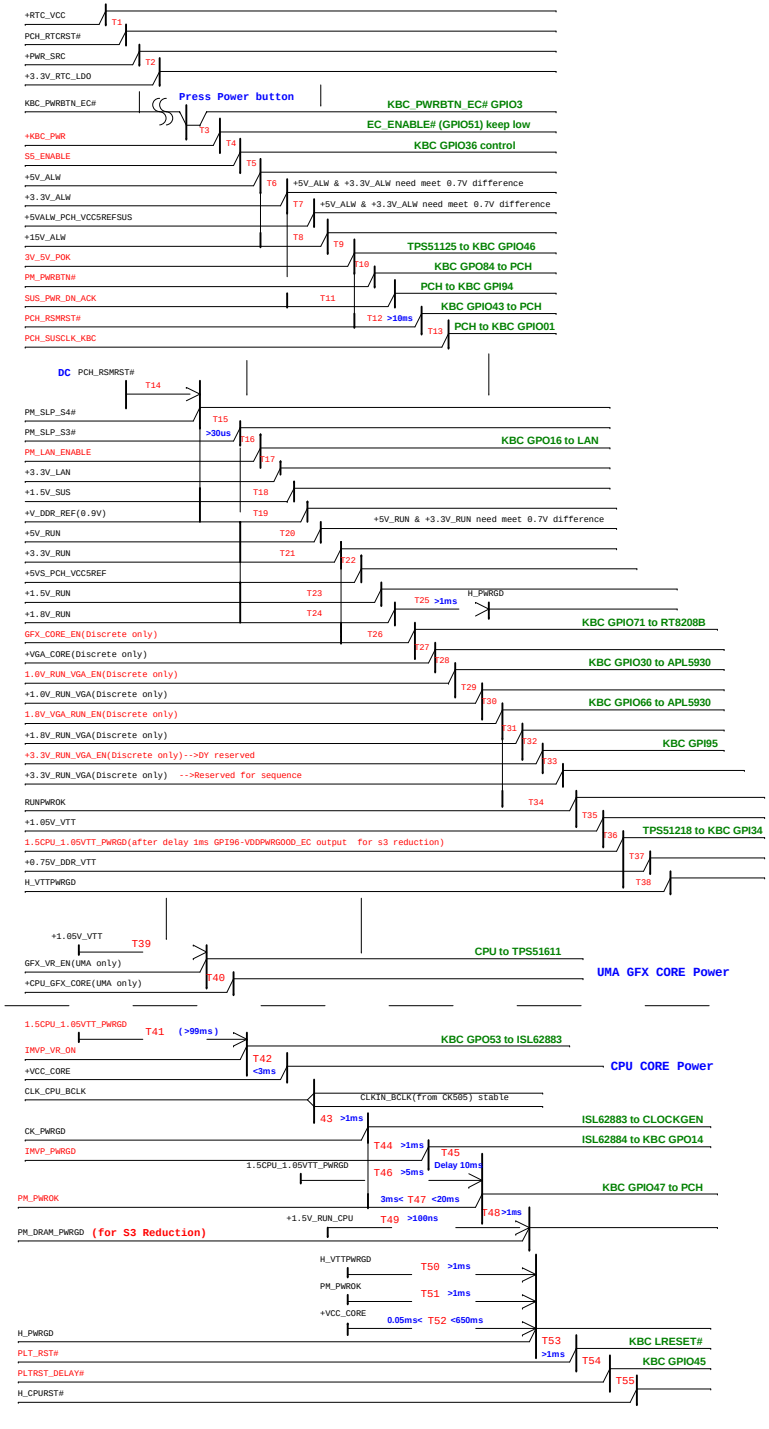
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence

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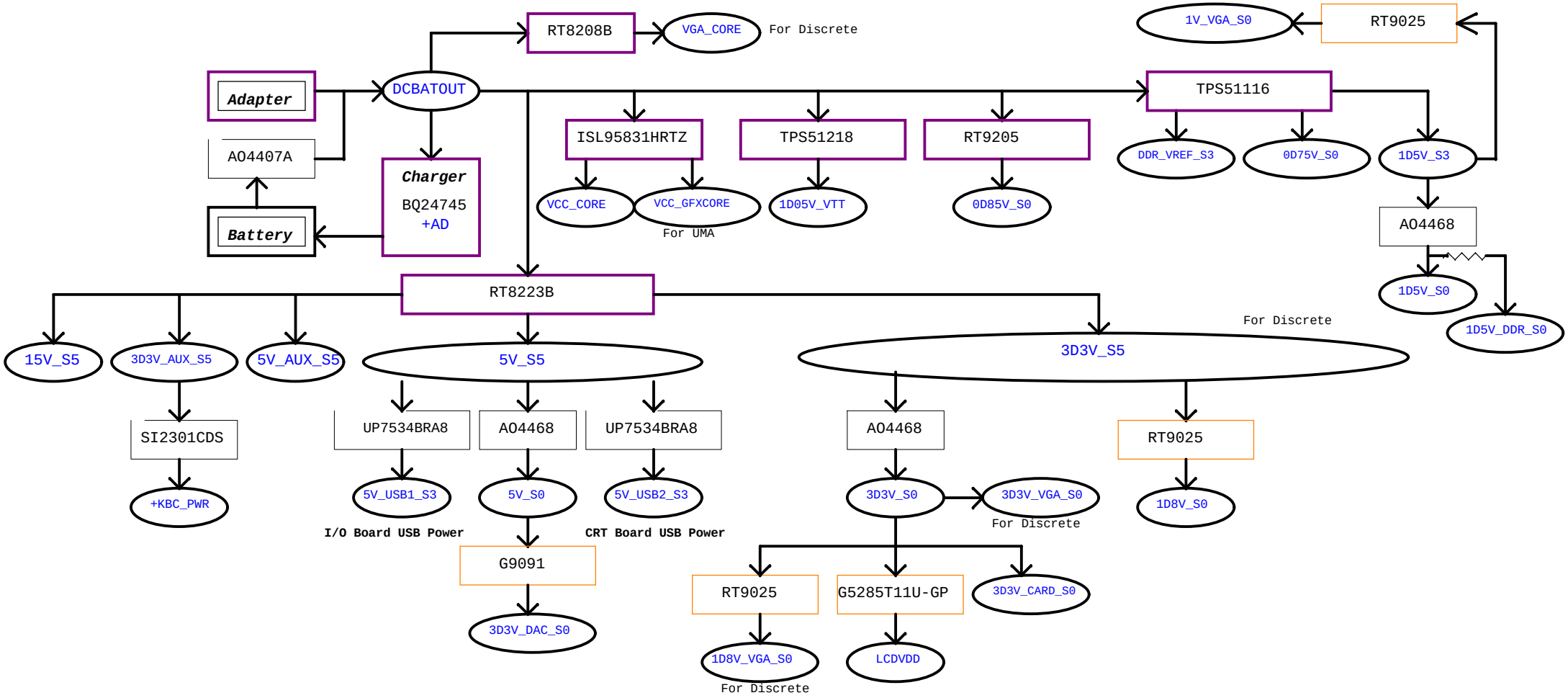
Not Update



Power Shape

Regulator	LDO	Switch

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Title: ***Power Block Diagram***

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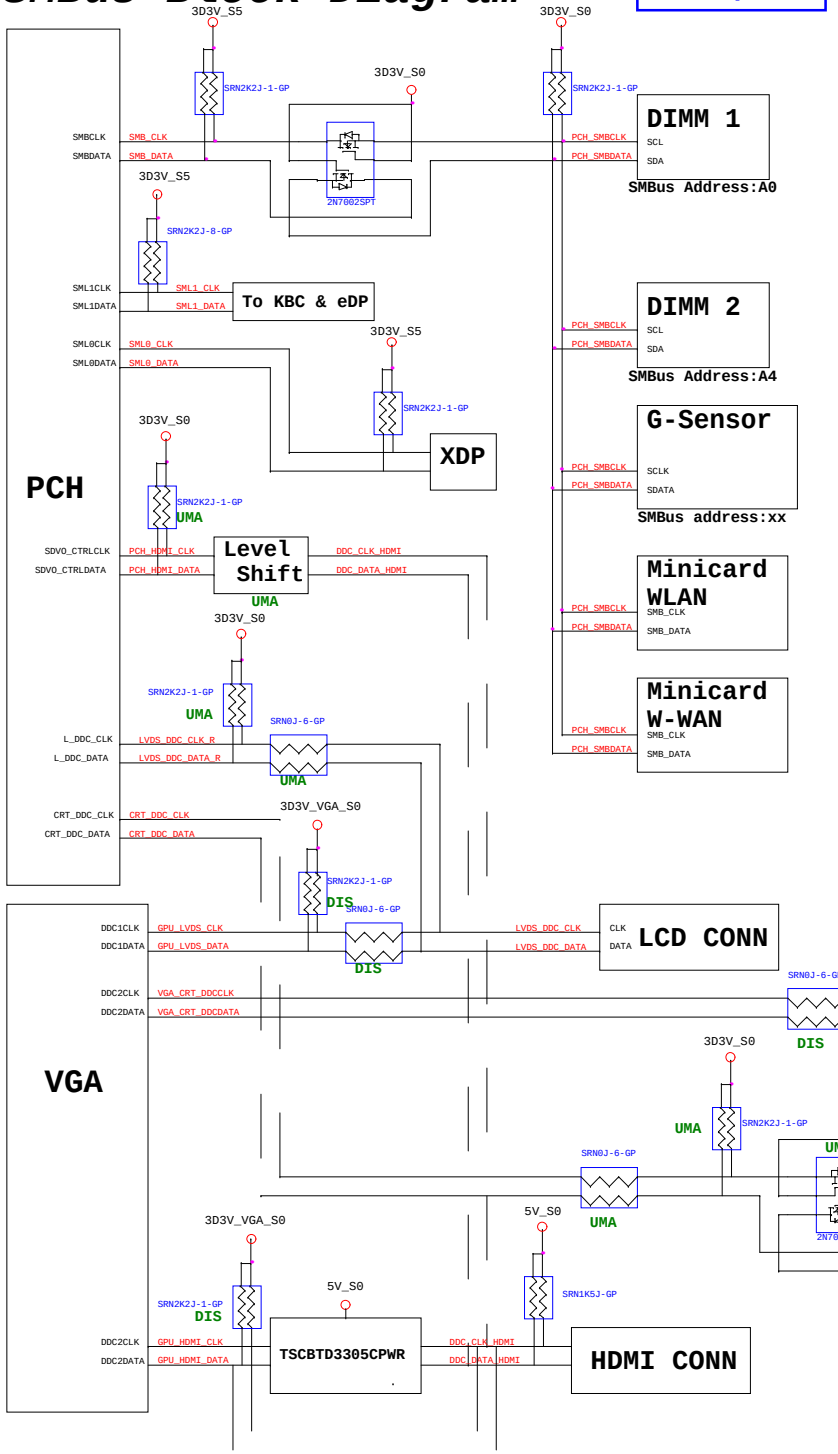
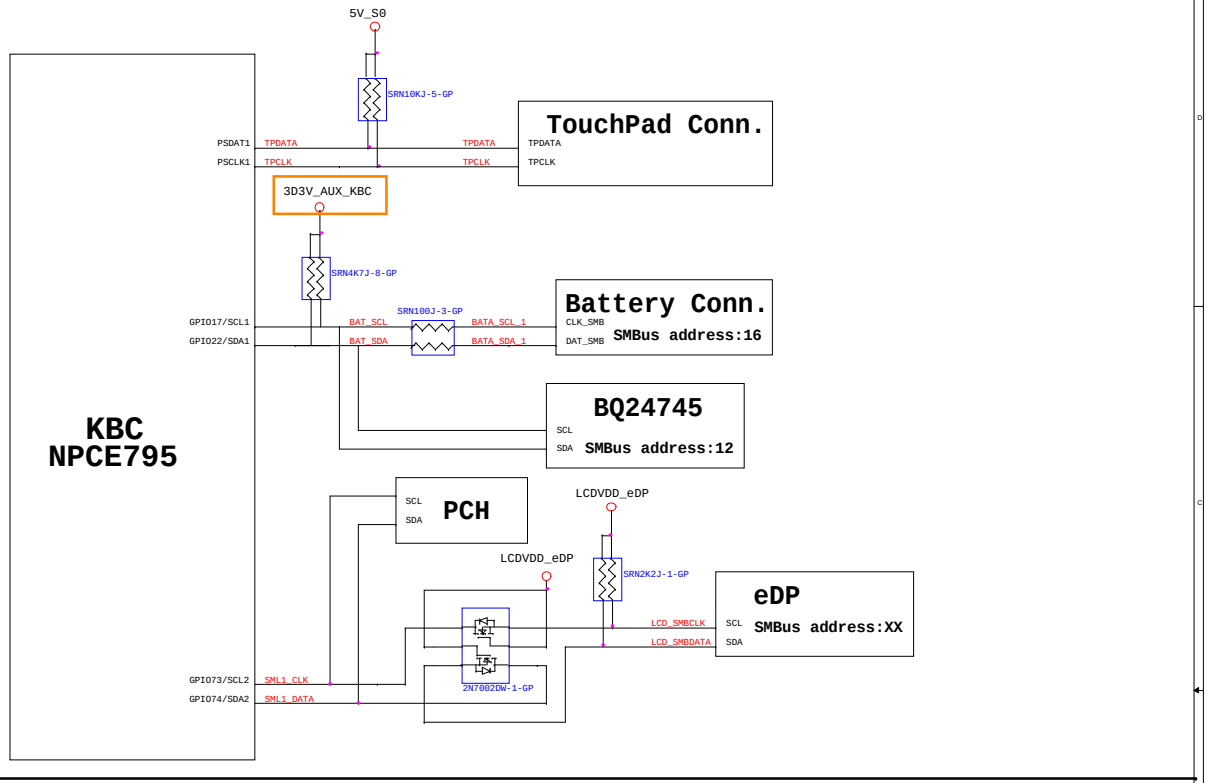
PCH SMBus Block Diagram

Not Update



KBC SMBus Block Diagram



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Title	SMBUS BLOCK DIAGRAM		
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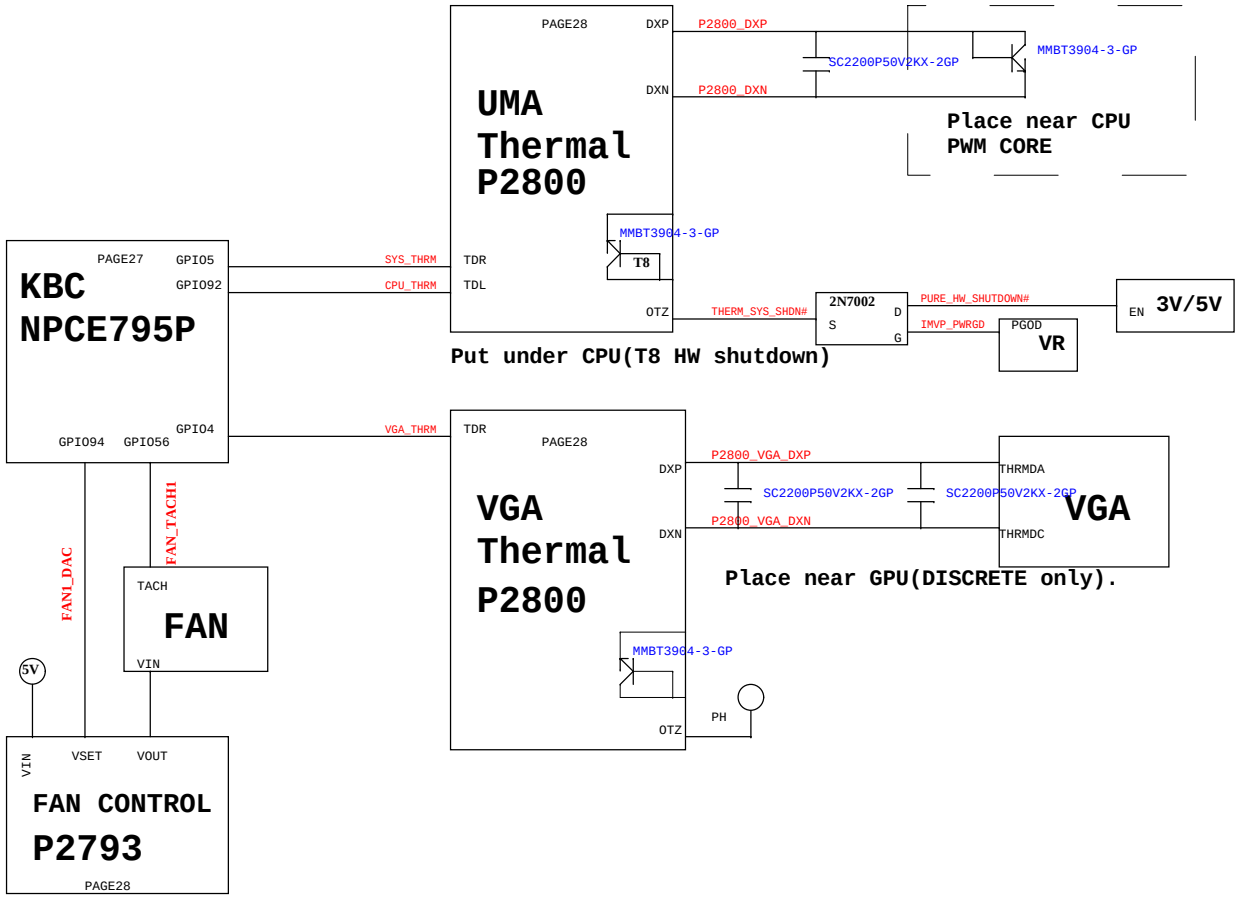
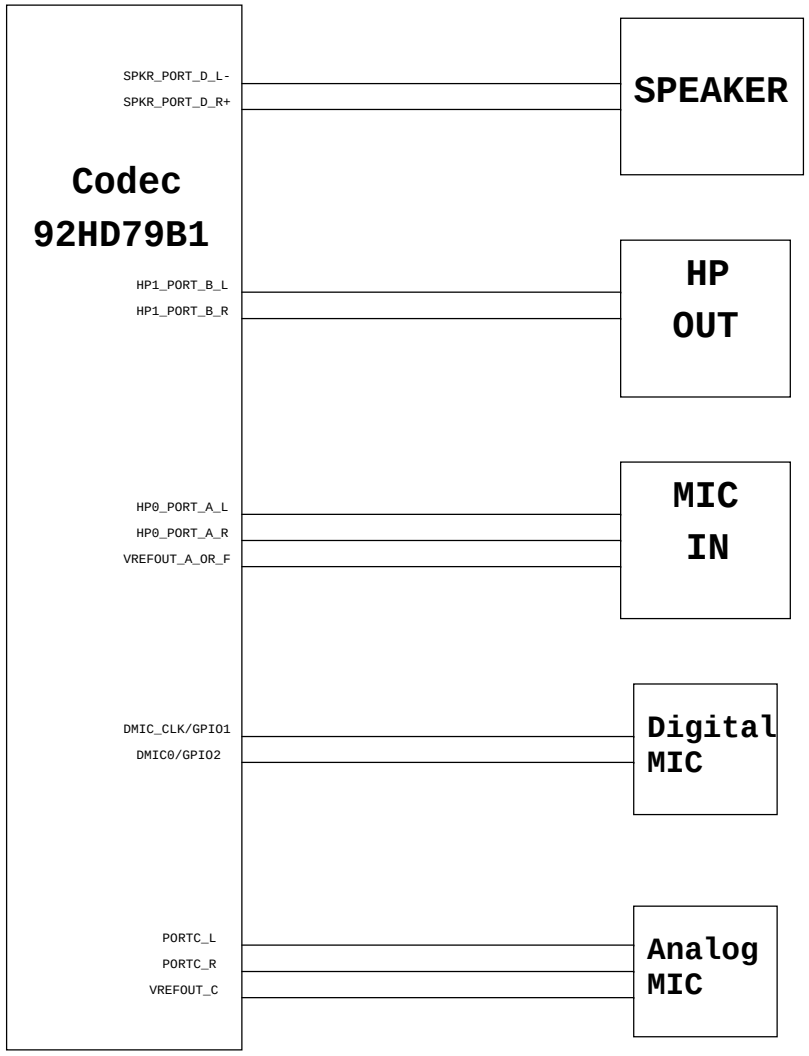
Thermal Block Diagram

Not Update



Audio Block Diagram



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Title	THERMAL/AUDIO BLOCK DIAGRAM	
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